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MS-7C80

ATX
Ver: 1.1

CML Platform

CPU:

Comet lake S 65W

Onboard Chip

HD Audio Codec: ALC1200

LAN Intel RTL8125B

LAN Intel I219

Flash ROM SPI 128MB X1

SIO NIC6687

Main Memory:

DDR4 (2666MHz) * 4 (Dual Channel)

PWM

NCP81229

ACPI

LDO

Expansion Slots:

PCI Express (X16) Slot * 1

PCI Express (X4) Slot * 1

PCI Express (X1) Slot * 2

M2 Slot * 2

System Chipset:

Z490 PCH_H

VGA Output:

HDMI Port

DP Port

Other:

SATA30 * 4

USB20 * 2

REAL USB3.1 Gen2 Type A

REAL USB3.1 Gen3 Type C

REAL USB3.1 Gen1 LAN_USB

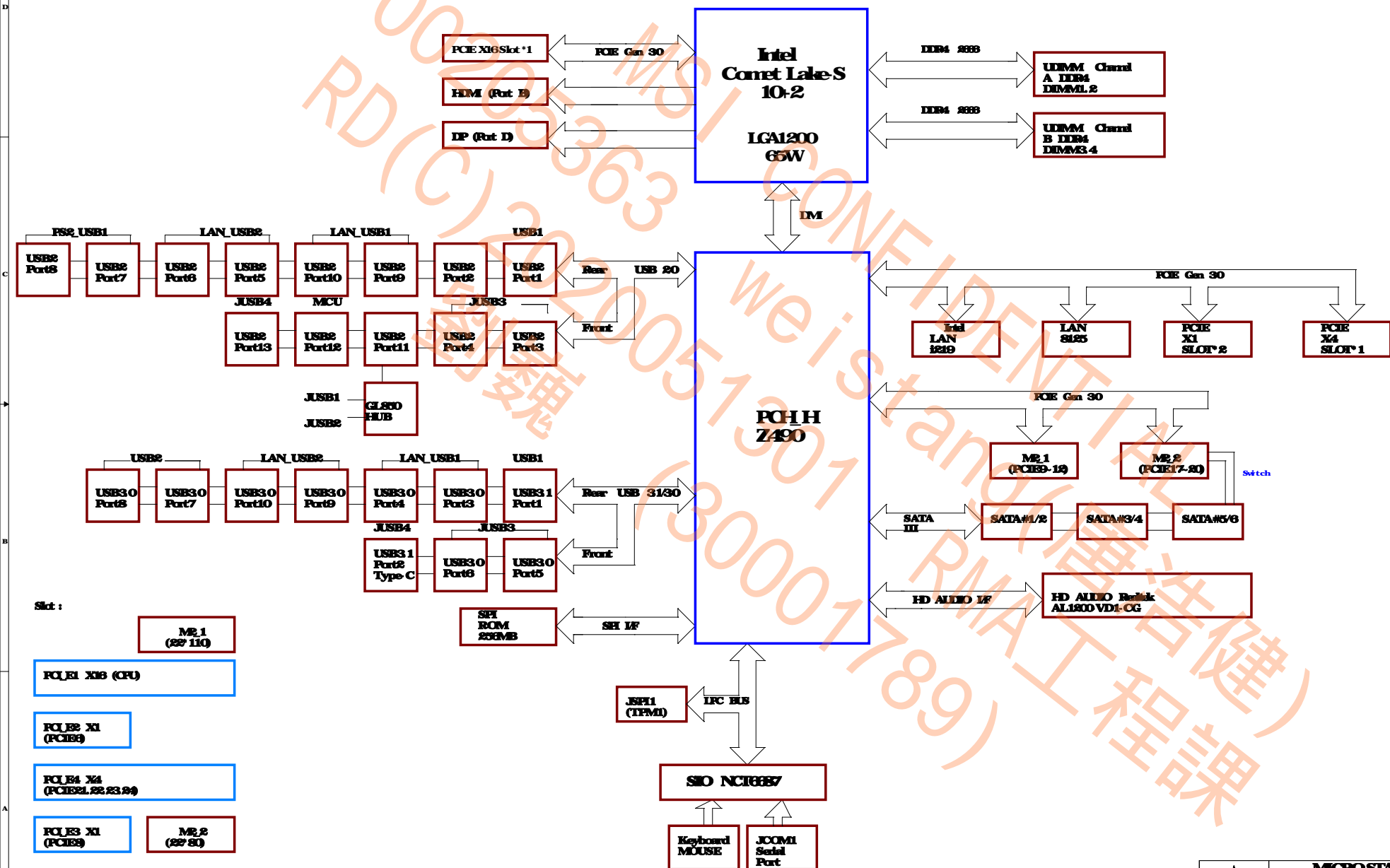
FRONT USB3.1 GEN1 TypeC

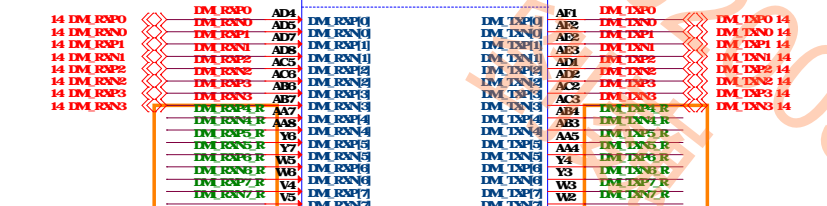
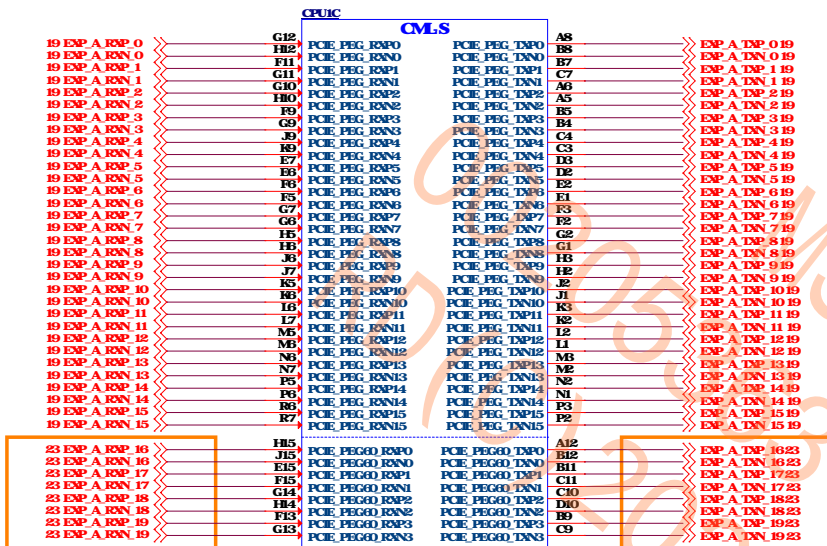
FRONT USB3.1 * 2



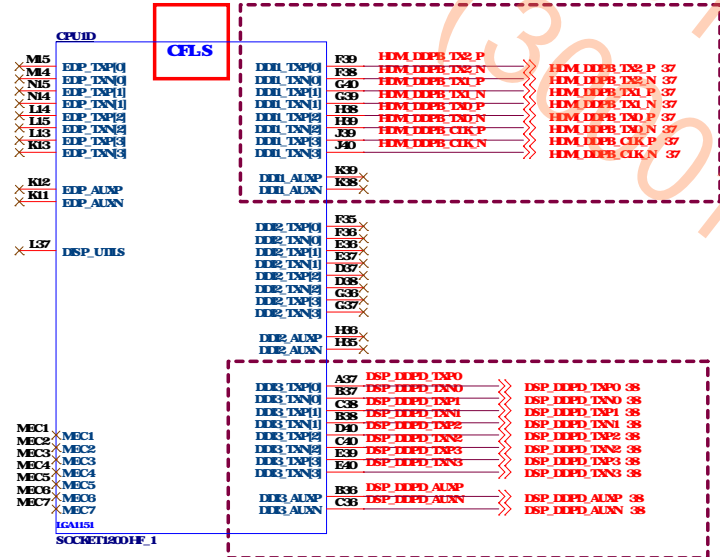
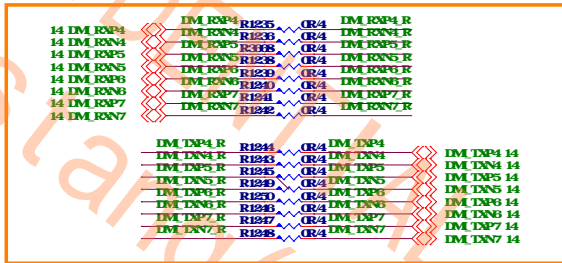
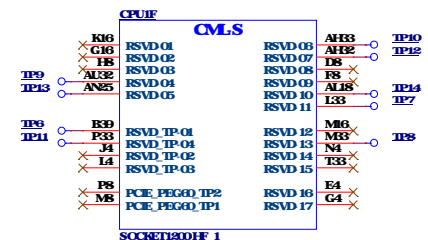
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MS-7C80			
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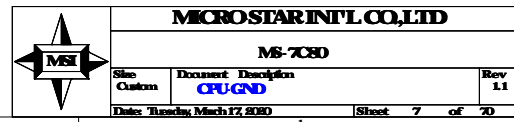
MS-7C80 Block Diagram

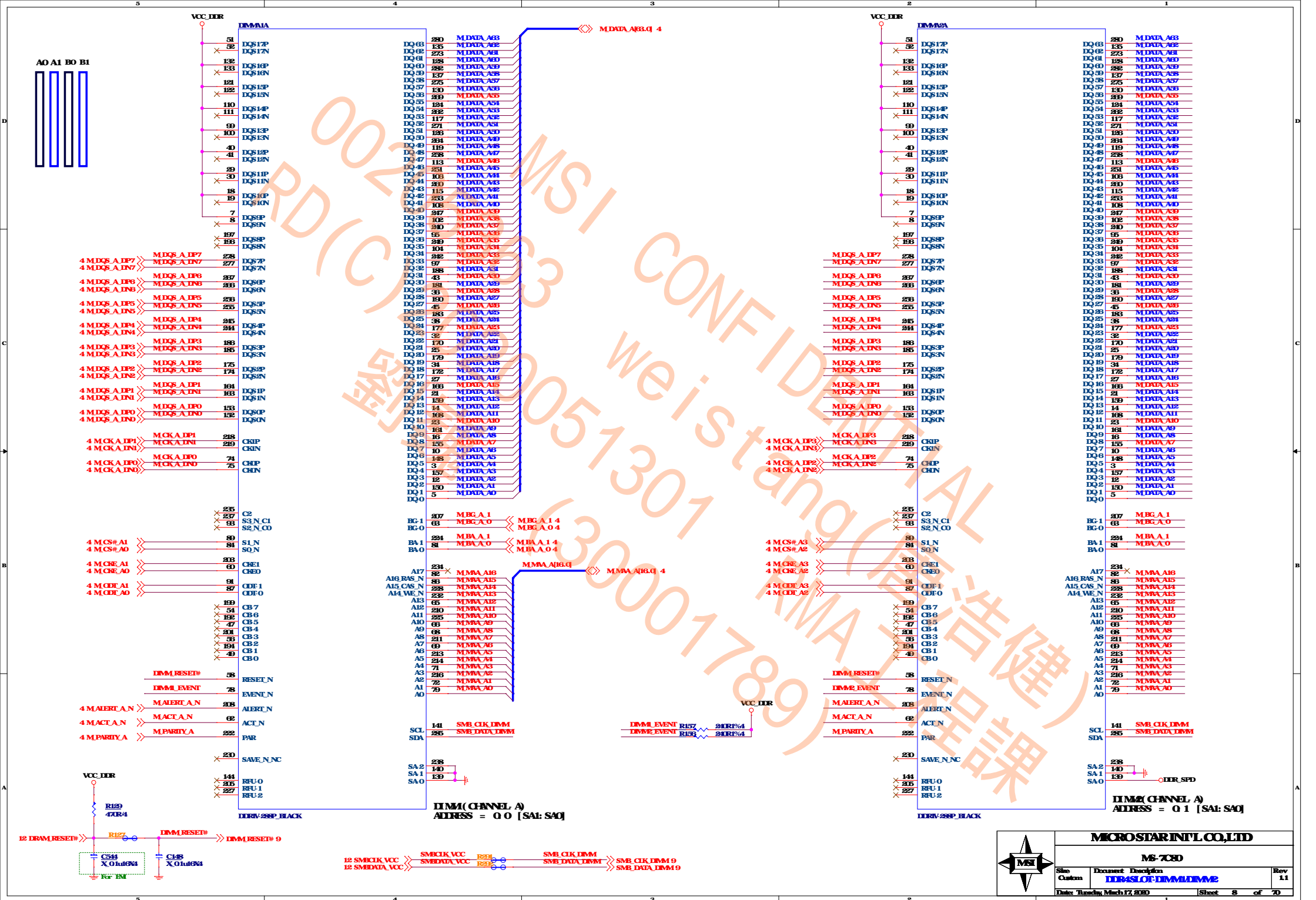


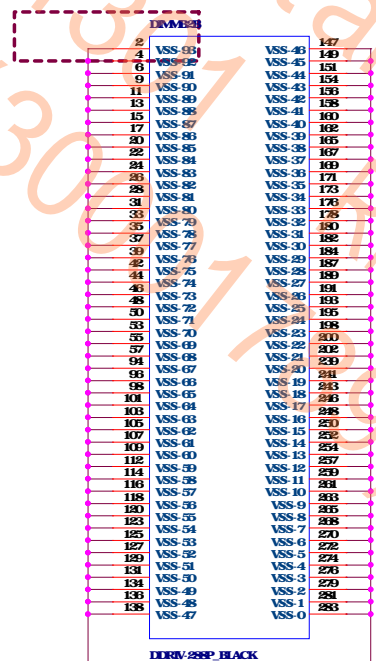
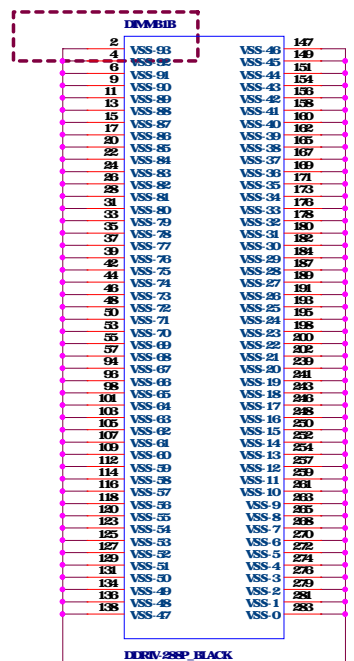
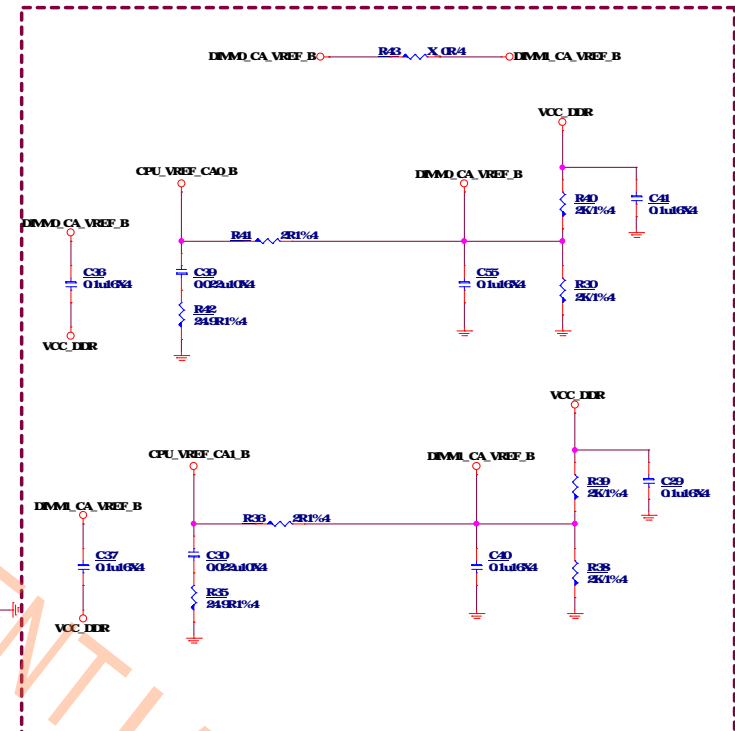
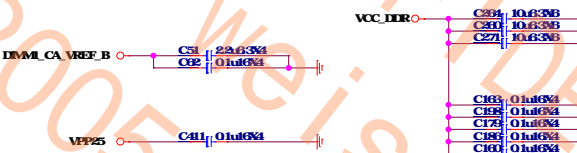
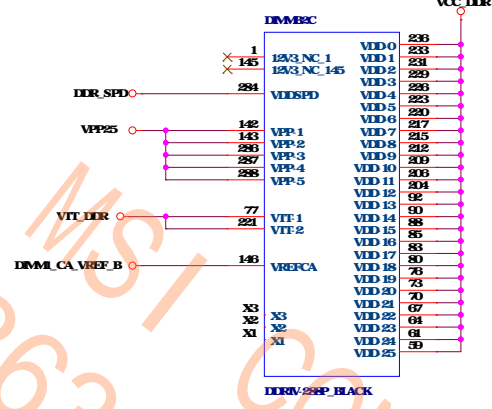
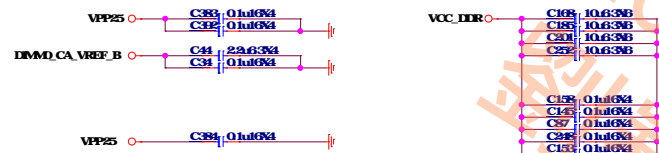
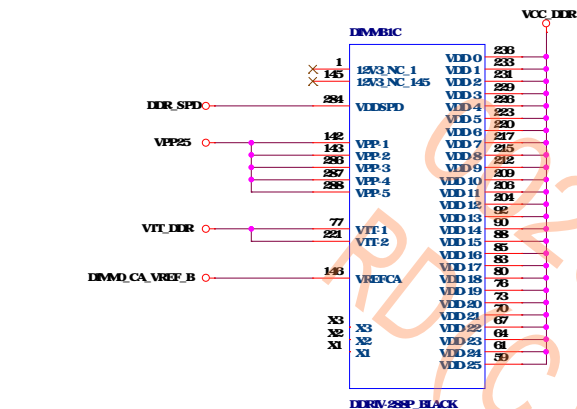


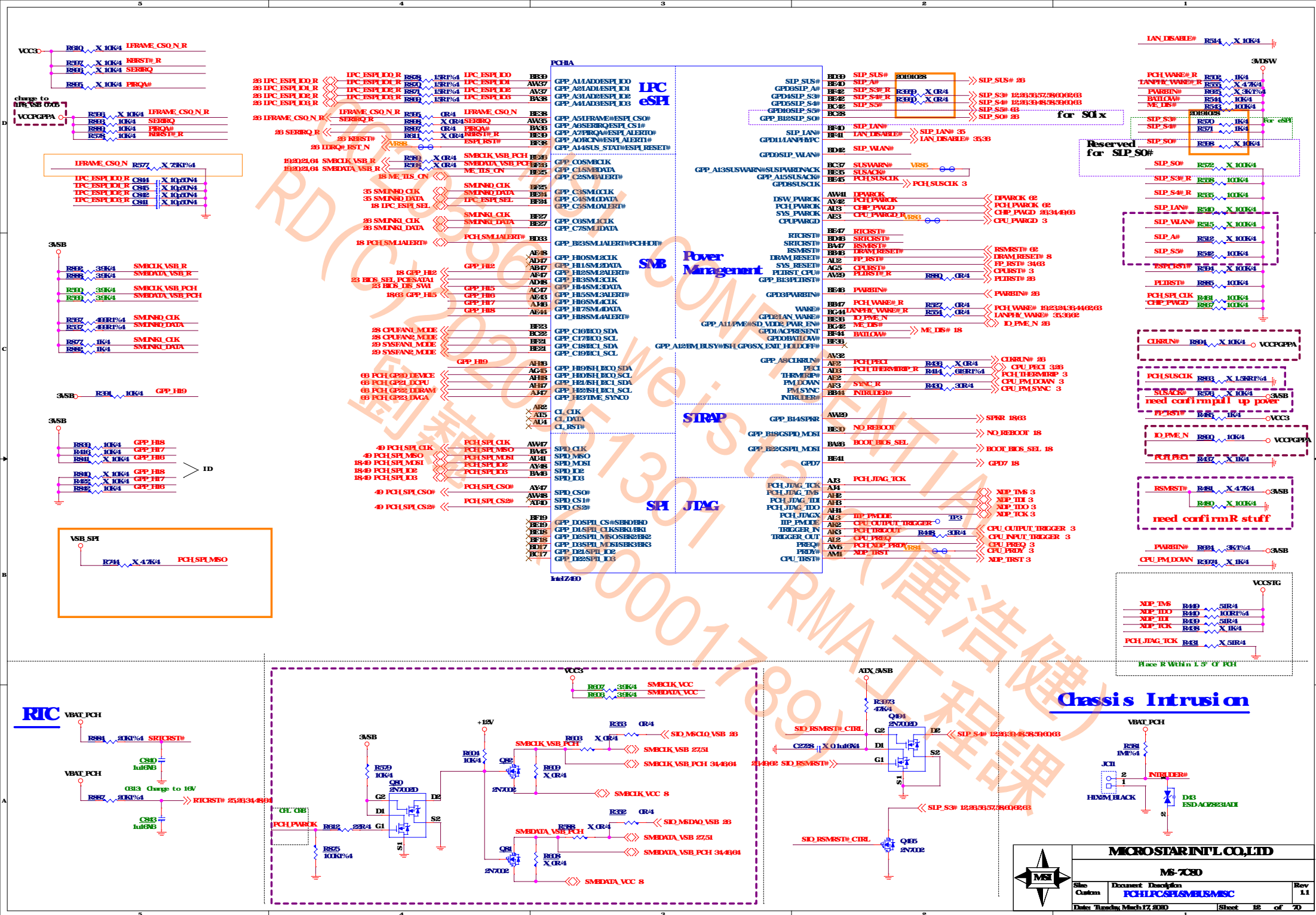
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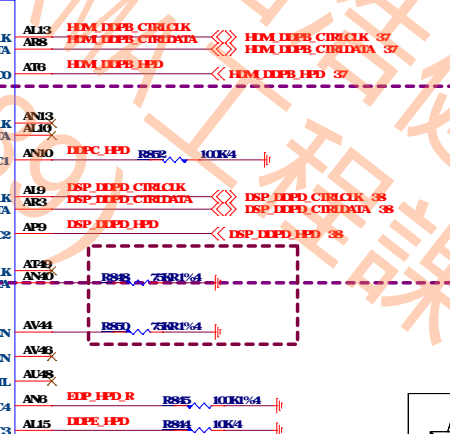
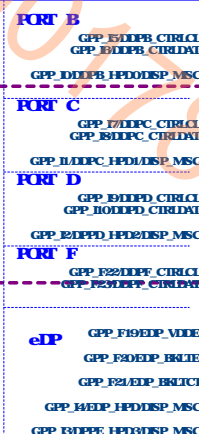
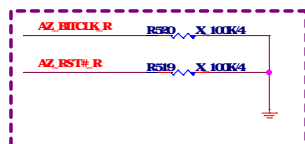
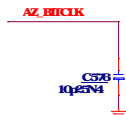
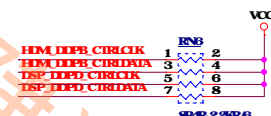
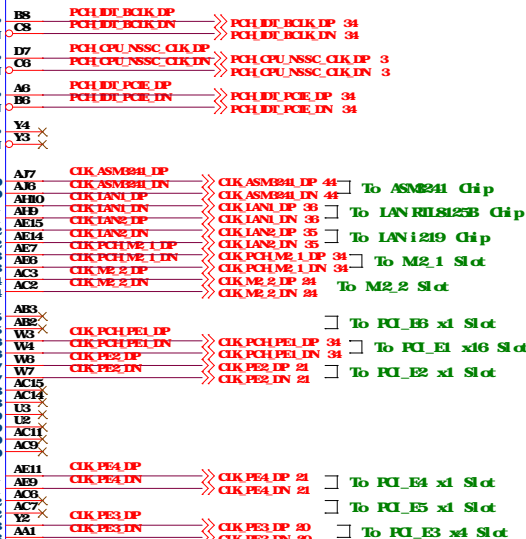
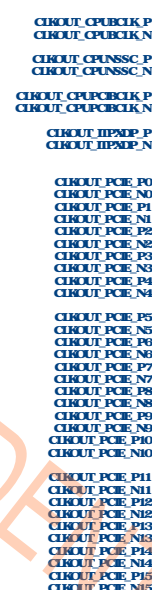
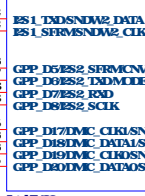
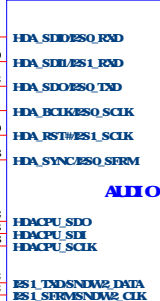
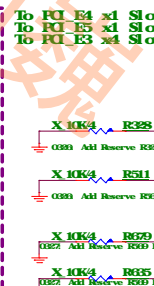
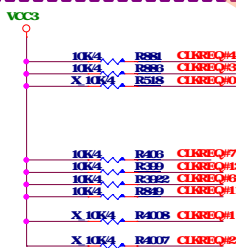
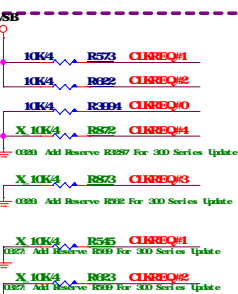
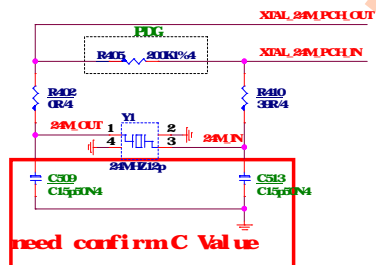
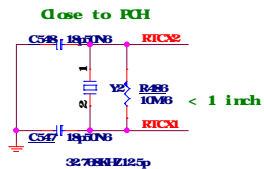


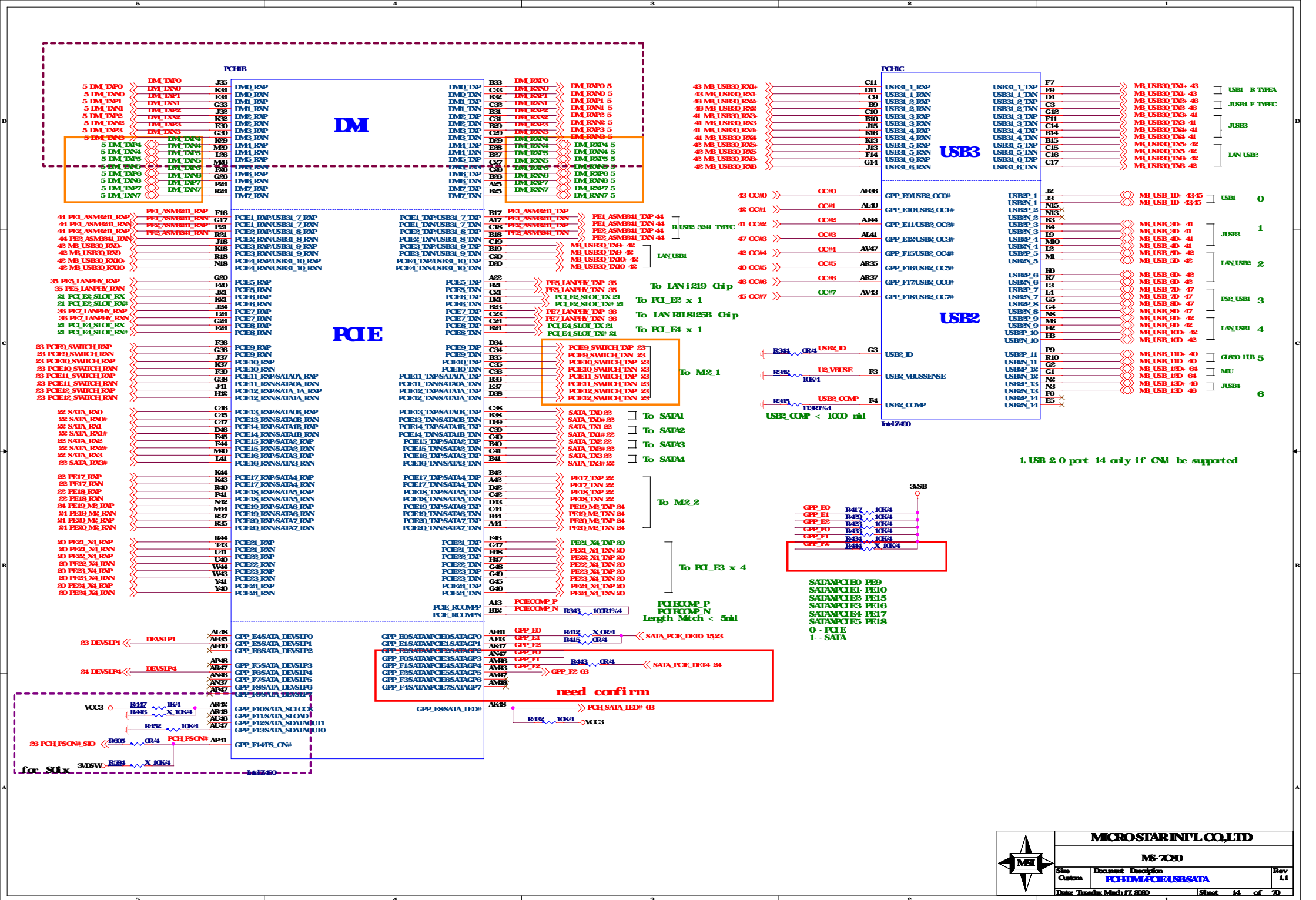


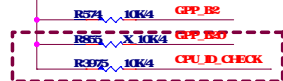
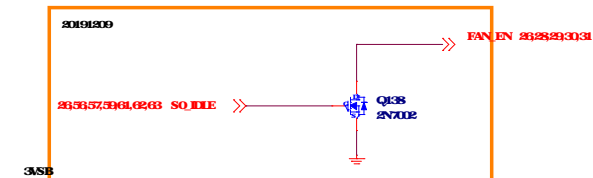




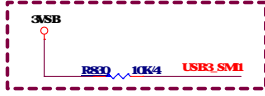
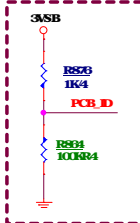






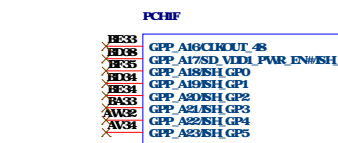
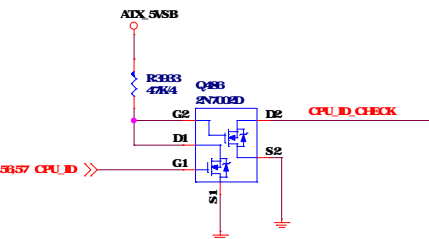


Use Acid S5 Leakage



PCH_IP8_VSB

CIO_GATE#



3V3B SIO_PROCHDI#



3V3B SIO_PROCHDI#

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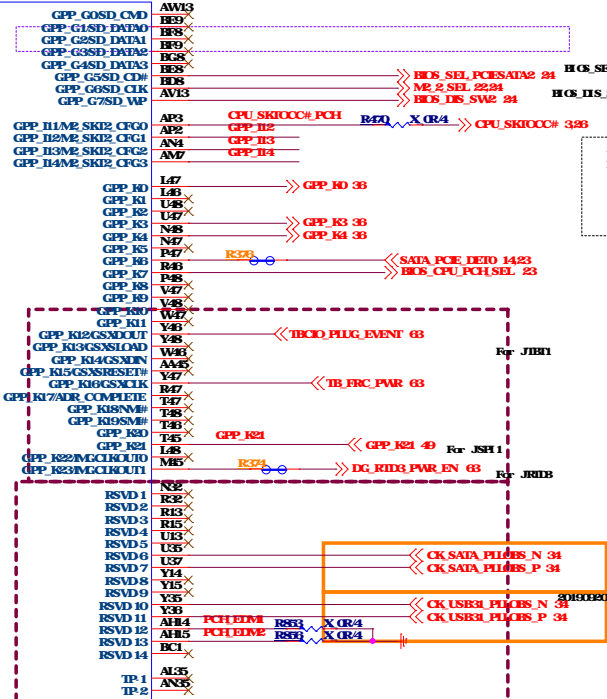
3V3B SIO_PROCHDI#

3V3B SIO_PROCHDI#



PCH

CNV



HOS Select

USE

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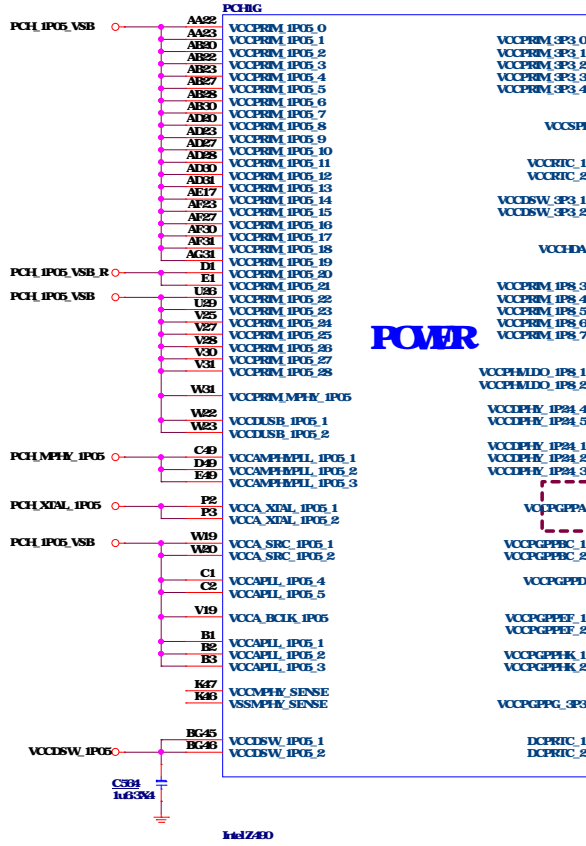
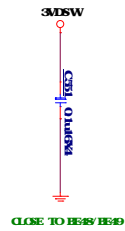
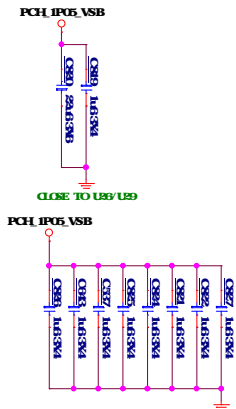
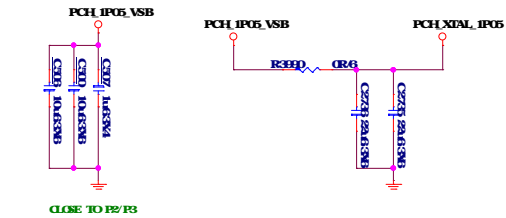
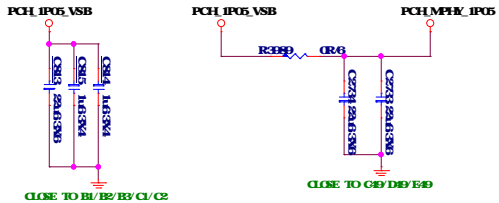
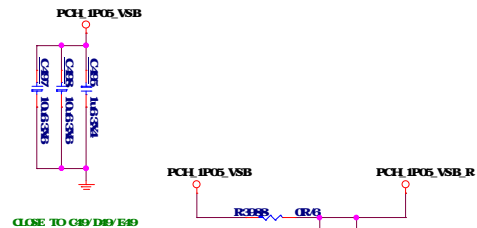
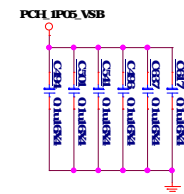


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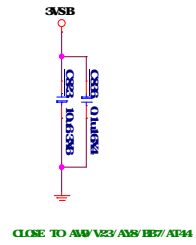
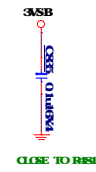
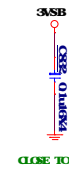
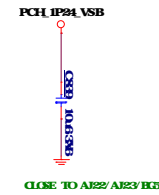
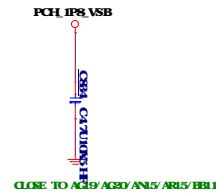
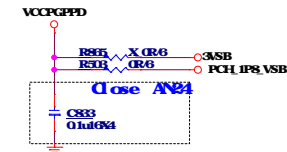
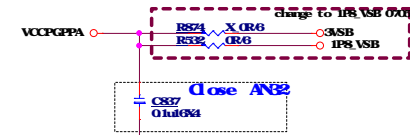
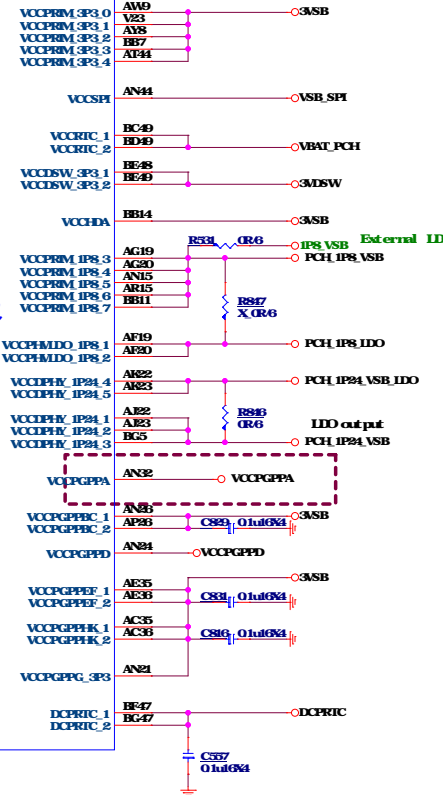
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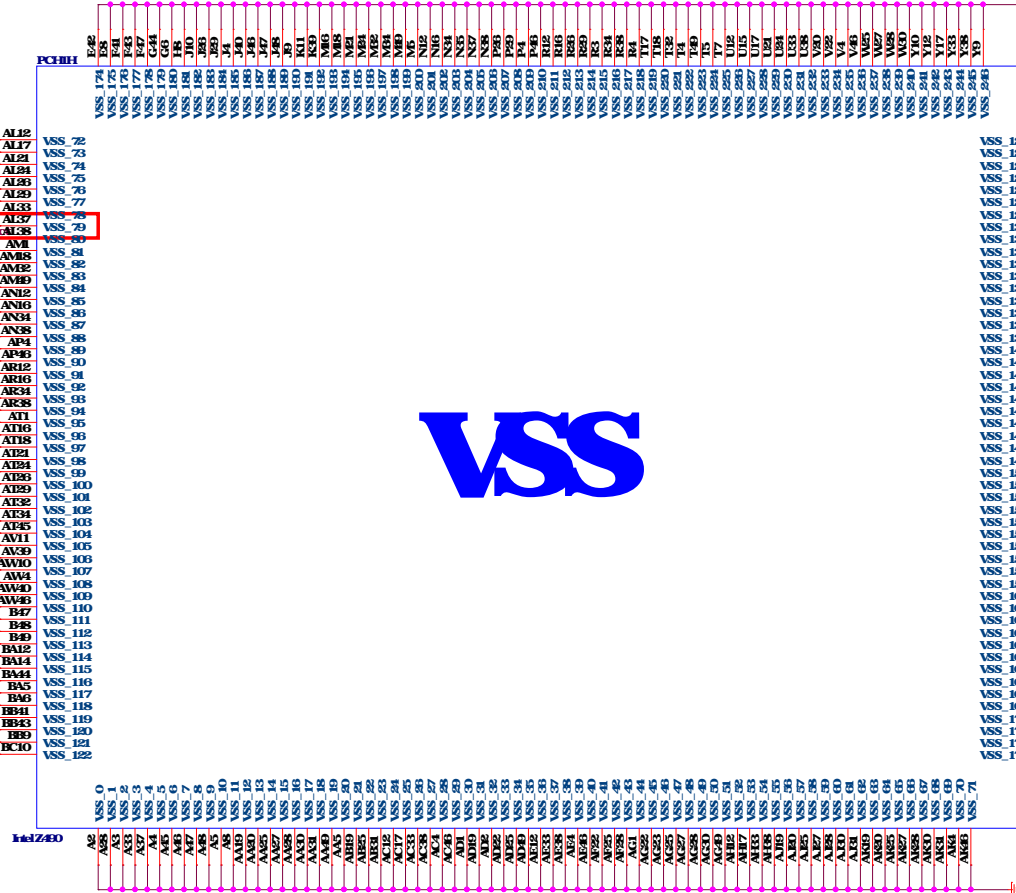


POWER

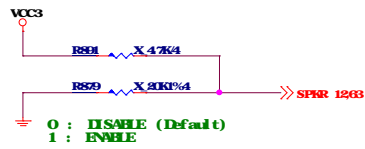


VSS

need confirm AL37

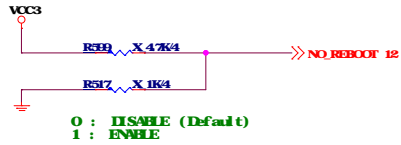


TCP Swap



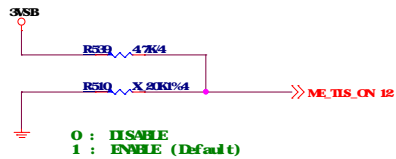
Internal Pull-down is disabled after PCHPMOK is High

No Reboot



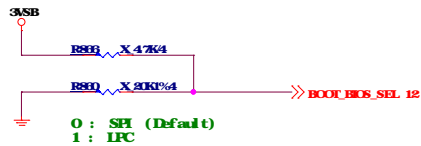
Internal Pull-down is disabled after PCHPMOK is High

TLS confidentiality



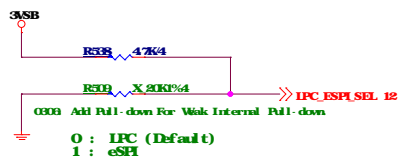
Internal Pull-down is disabled after RSMST# de-assert.

Boot HCS



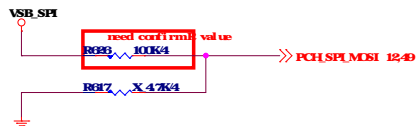
Internal Pull-down is disabled after PCHPMOK is High

LPC eSPI Mode

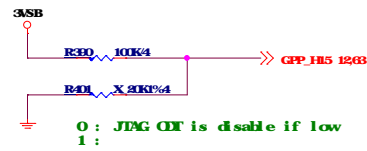


Internal Pull-down is disabled after RSMST# de-assert.

Reserved

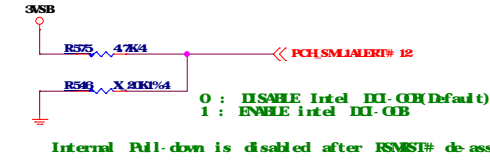


OT Disable



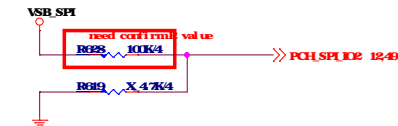
Internal Pull-down is disabled after RSMST# de-assert.

DI Enable

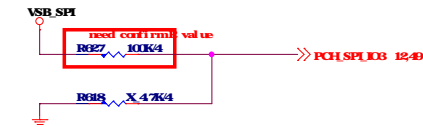


Internal Pull-down is disabled after RSMST# de-assert.

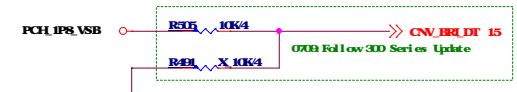
Reserved



Reserved

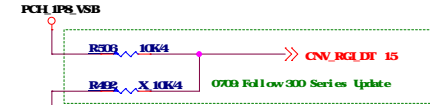


XIAL FREQUENCY SELECTION



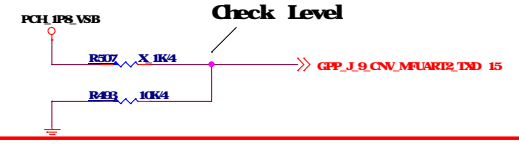
This Signal has a Weak Internal Pull-down.
An External Pull-up is Required On this Strap Since 38.4 MHz XIAL is Not Supported On the PCH.
0 = 38.4 MHz XIAL Frequency Selected (Default)
1 = 24MHz XIAL Frequency Selected

Midem Reference Clock Source Select



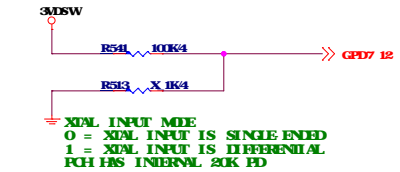
A Weak External Pull-up is Required
0 = Integrated CNA Enable
1 = Integrated CNA Disable

1.8V VCCSPH

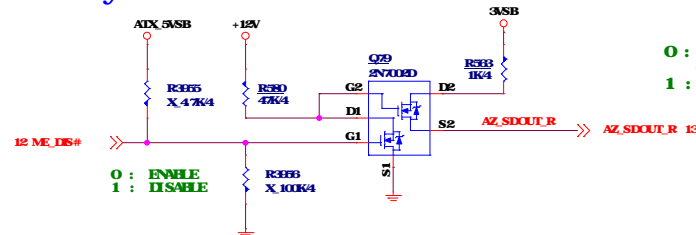


SELECT THE SPI BIOS FLASH INTERFACE OPERATING VOLTAGE
0 = VCCSPH IS CONNECTED TO 3.3V RAIL - DEFAULT
1 = VCCSPH IS CONNECTED TO 1.8V RAIL
PCH HAS INTERNAL 20K PD

Reserved



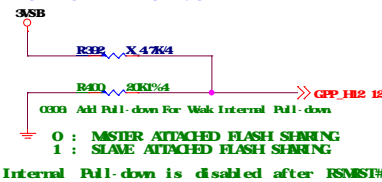
Flash Descriptor Security Override



0 : Enable security measures defined in the Flash Descriptor. (Default)
1 : DISABLE Flash Descriptor Security(Override).

Internal Pull-down is disabled after PCHPMOK is High

ESPI FLASH SHARING MODE



Internal Pull-down is disabled after RSMST# de-assert.



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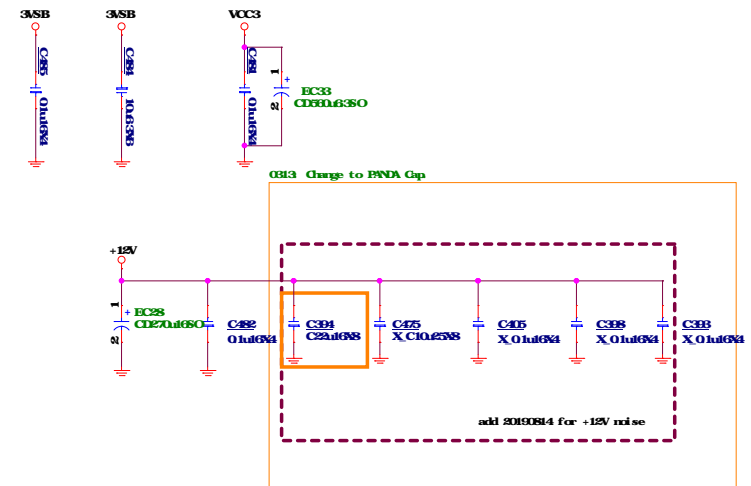
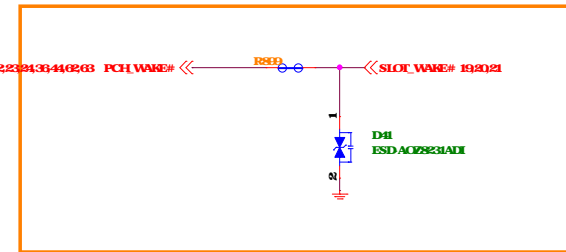
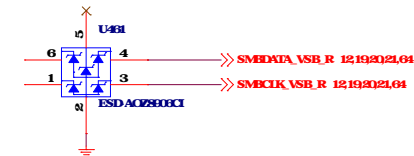
PCI_Express X16 Slot

12V - 5 5A

VOC3 - 3A

3VSB 375nA

SMBus ESD



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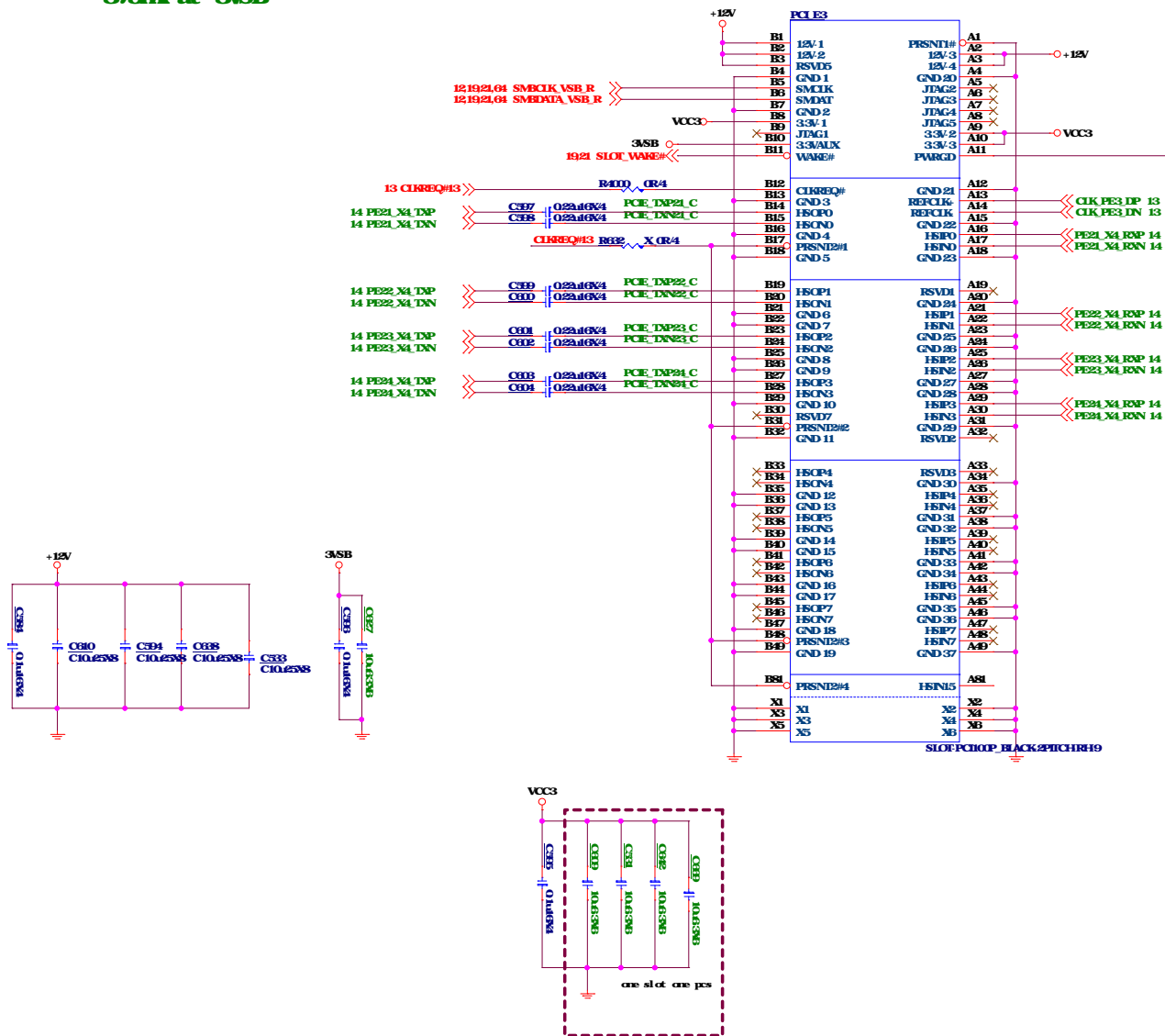
Date: Tuesday, March 17, 2020

Rev
1.1

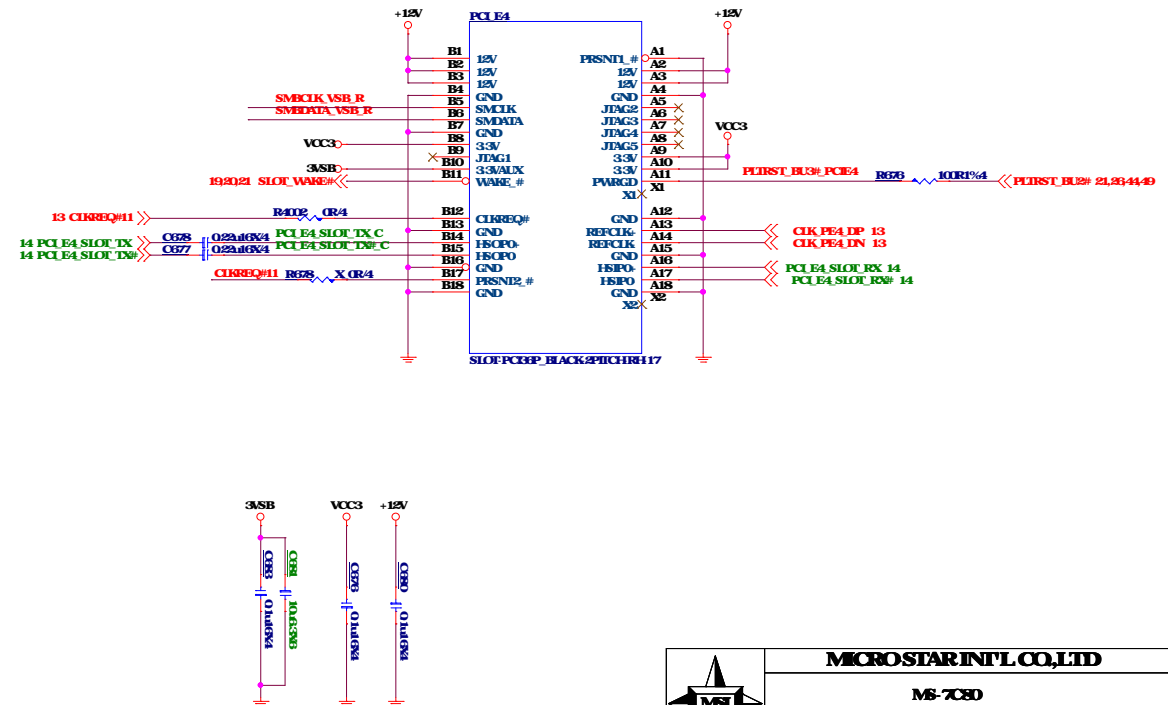
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PCI_Express X4 Slot

2 1A at +12V
3A at VCC3
375mA at 3VSB



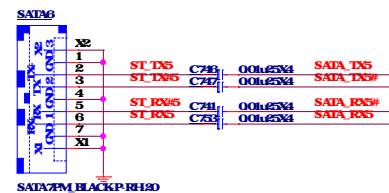
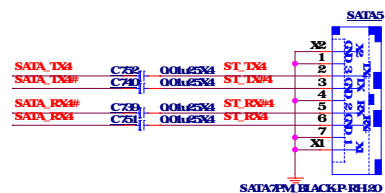
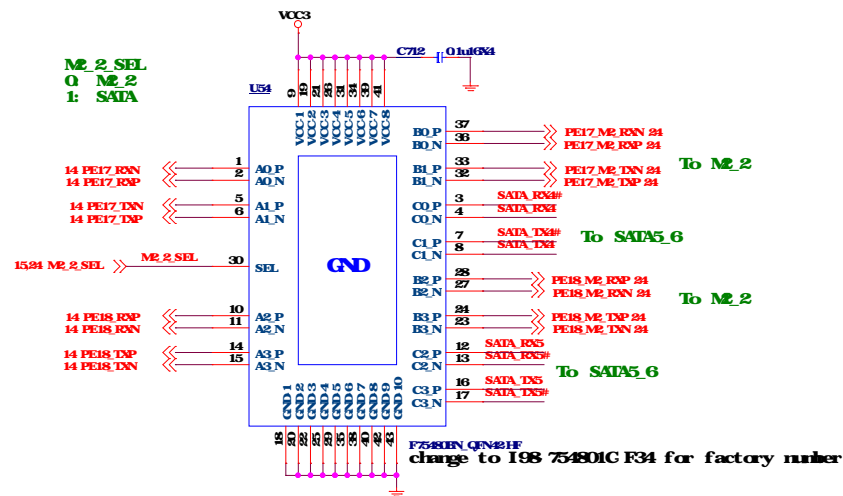
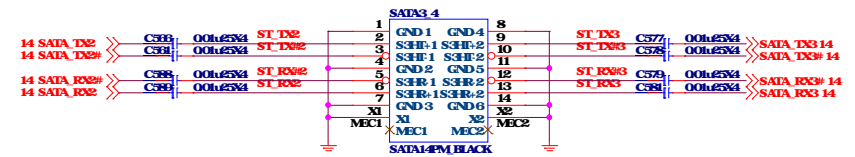
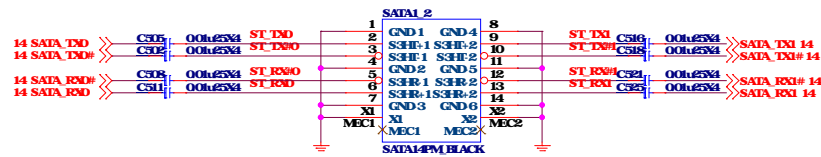
12V - 0.5A
VCC3 - 3A
3VSB - 375mA



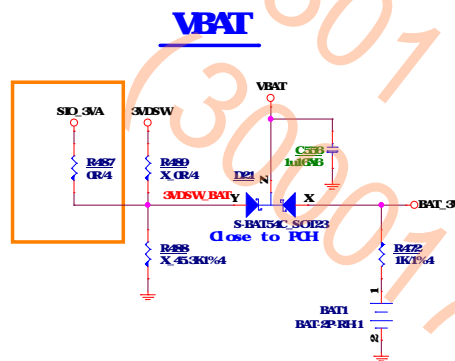
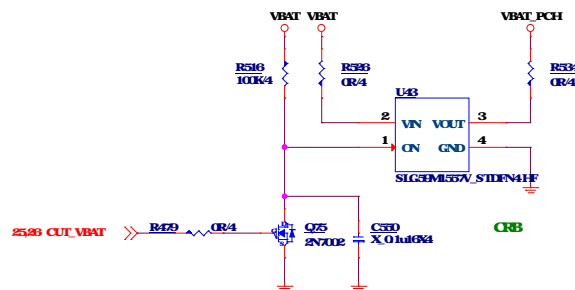
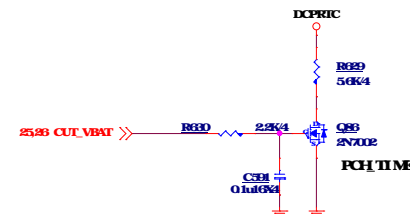
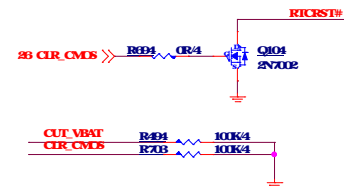
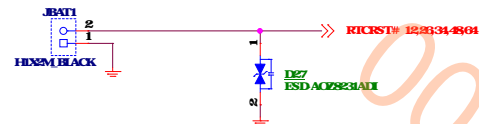
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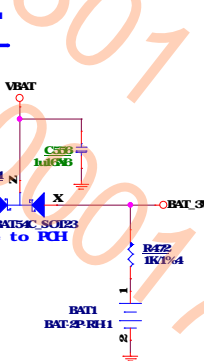
SATA Connector



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VBAT

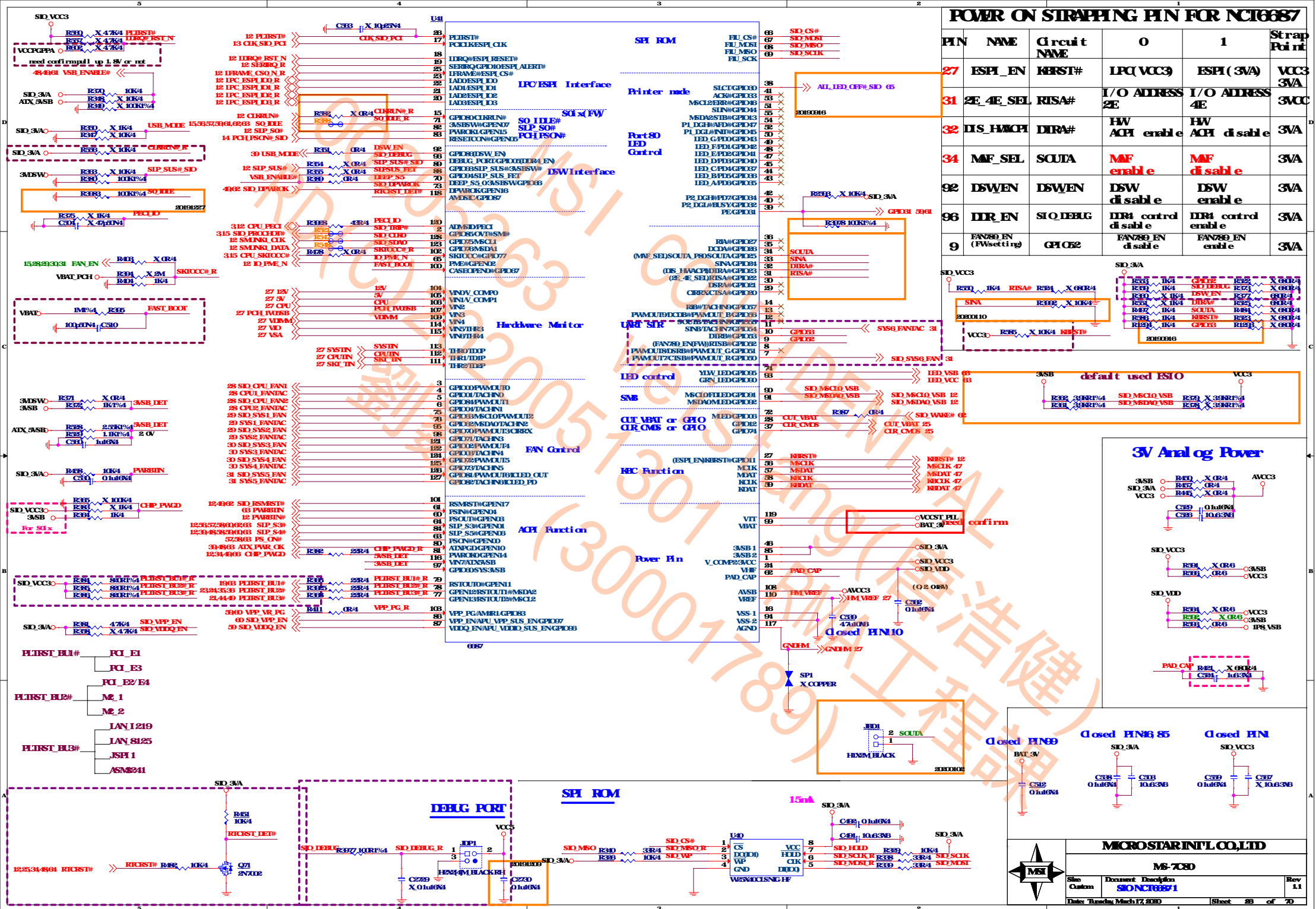


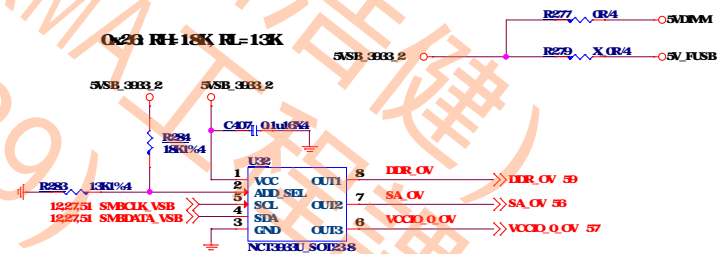
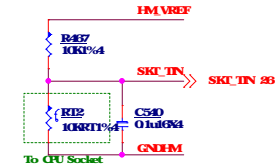
MICROSTAR INT'L CO., LTD

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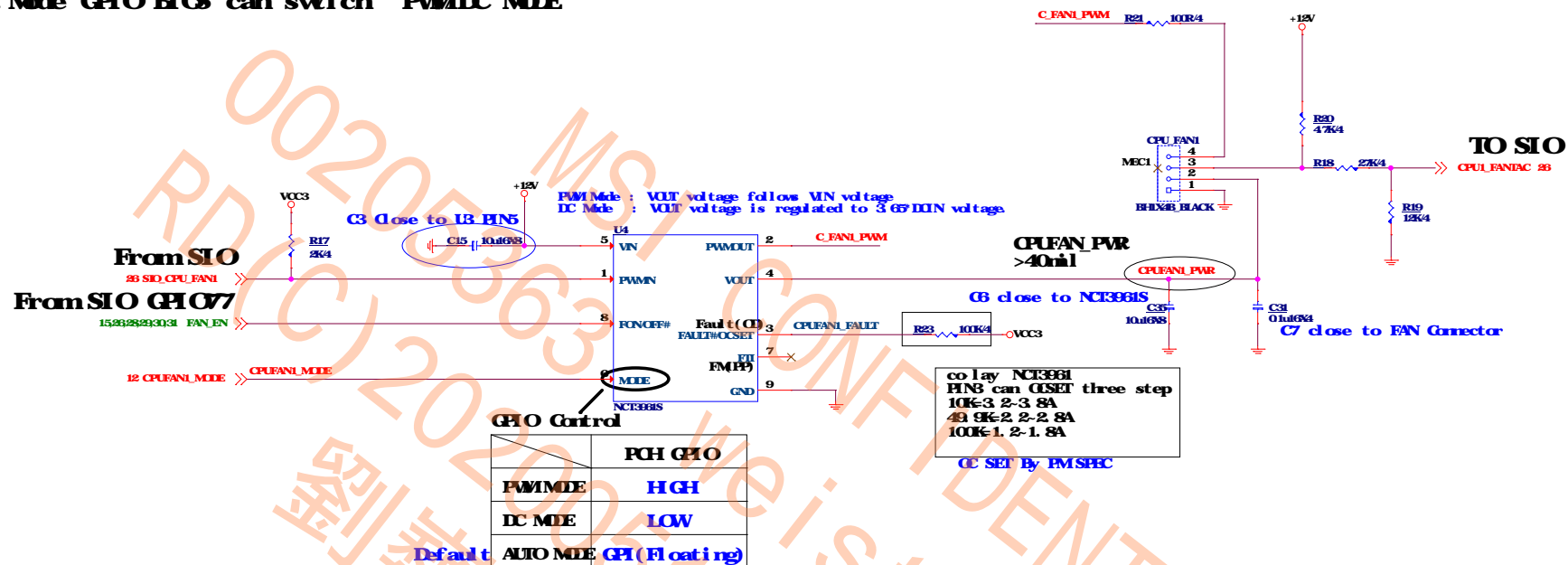


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1.1

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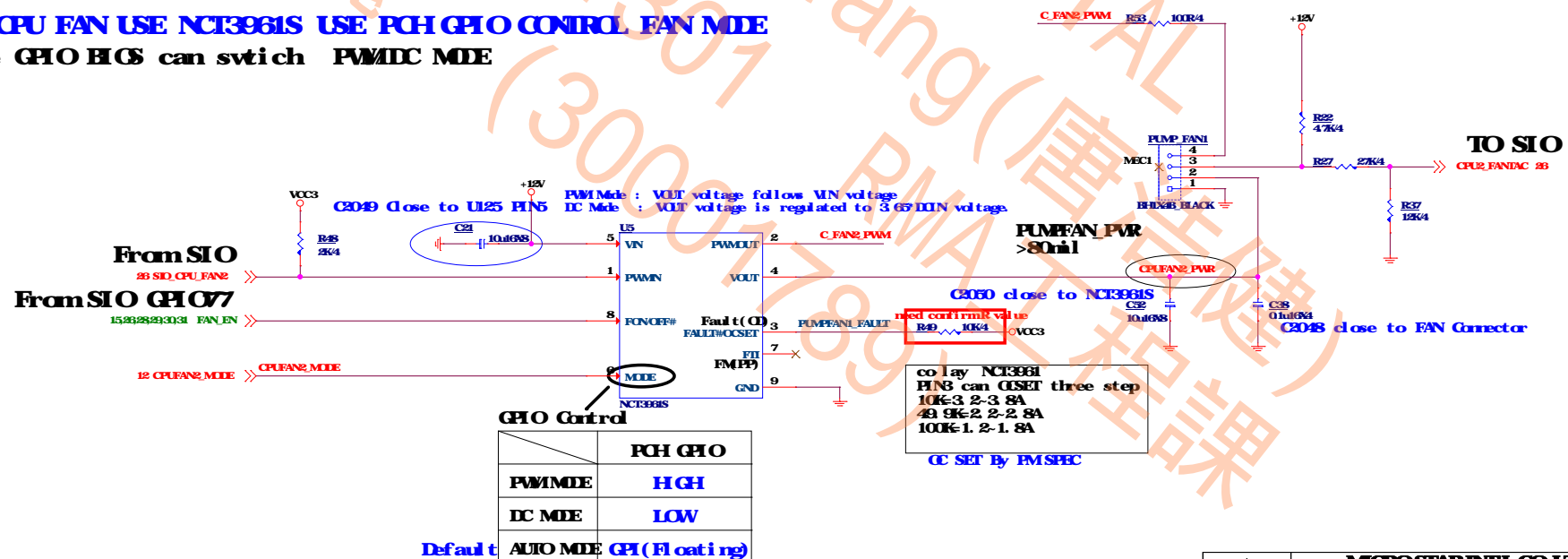
TYPE M: 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1. Mode GPIO HCS can switch PWM/DC Mode



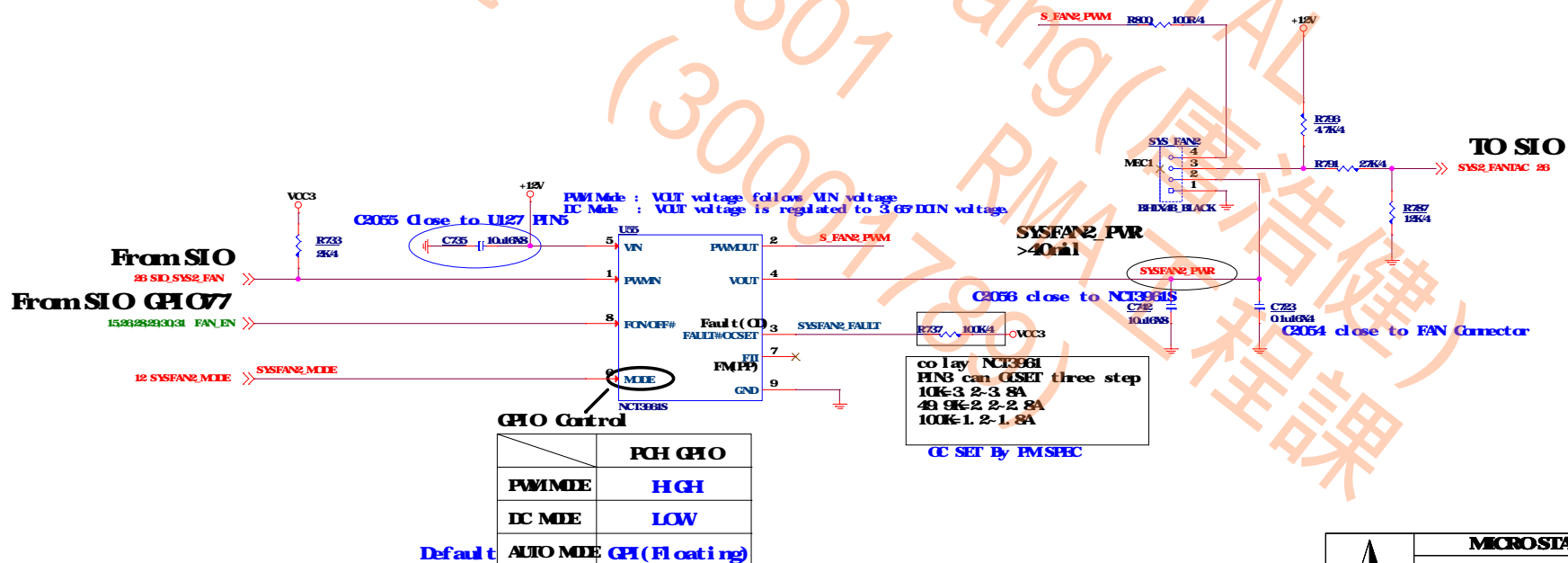
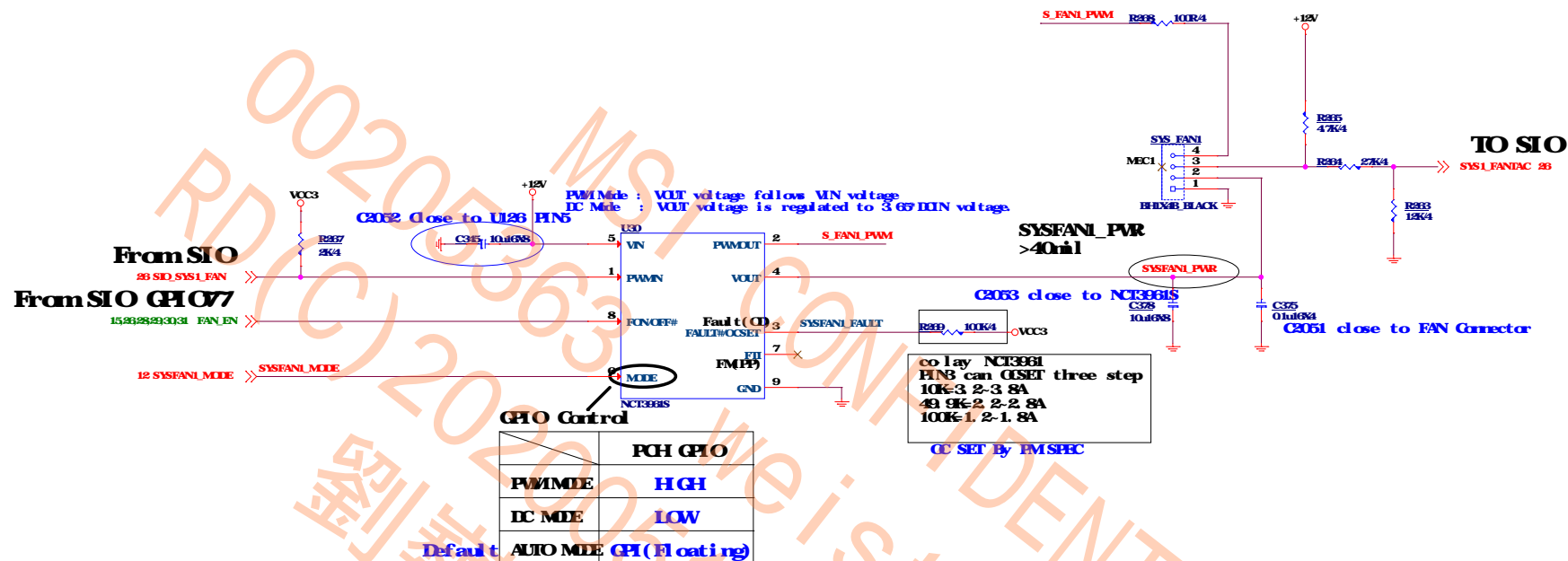
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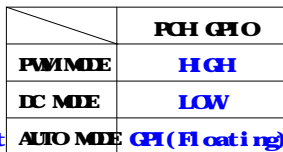
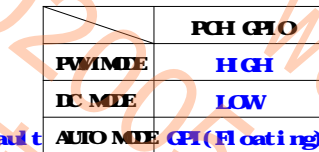


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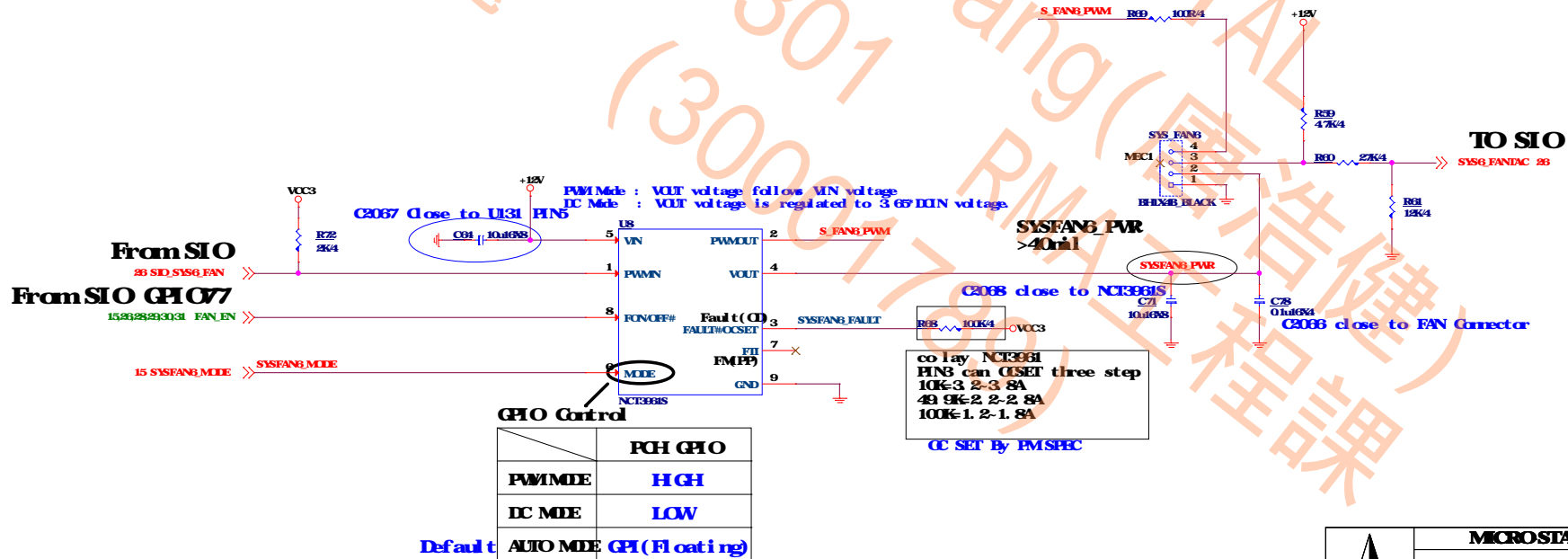
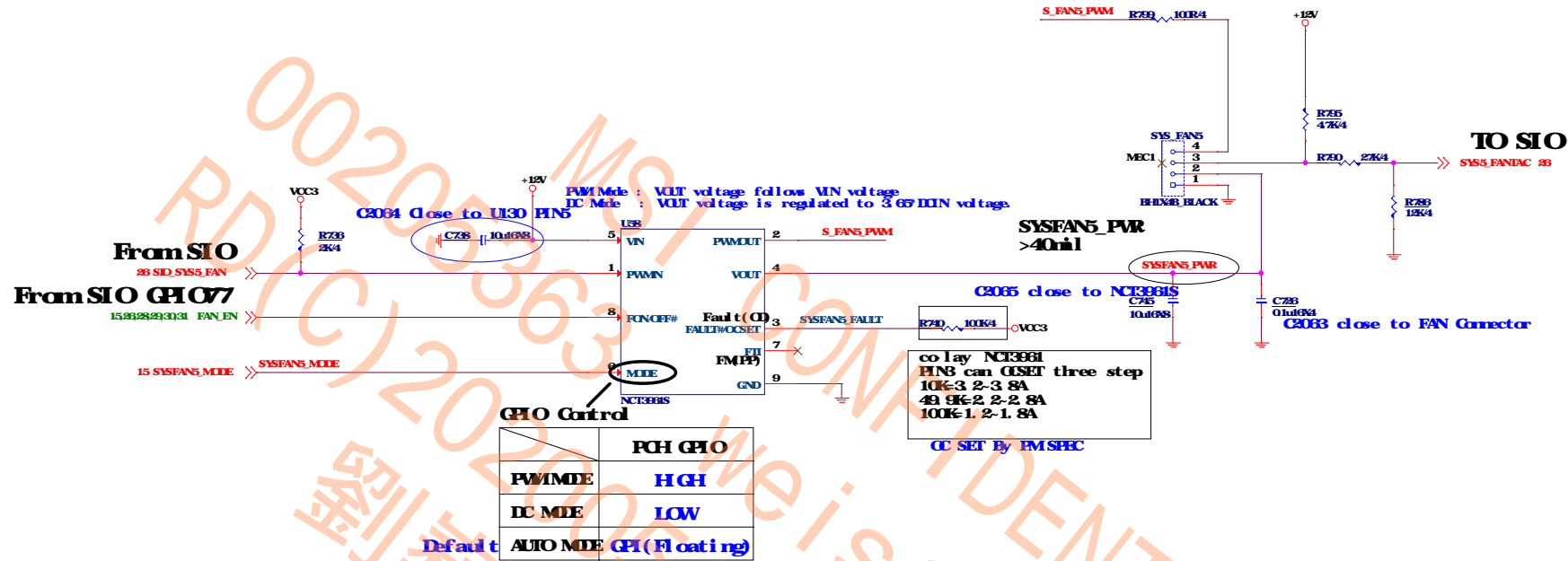


1. Mode GPIO HCS can switch PWMDC MODE



TYPE M: 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MDE

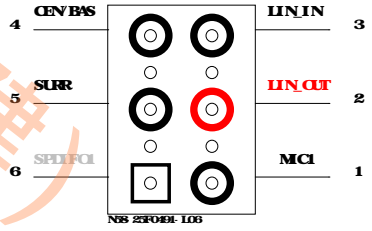
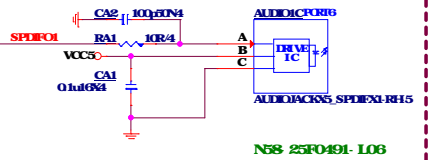
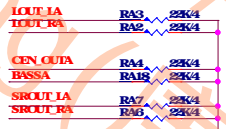
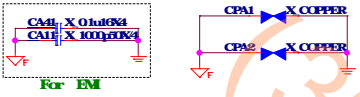
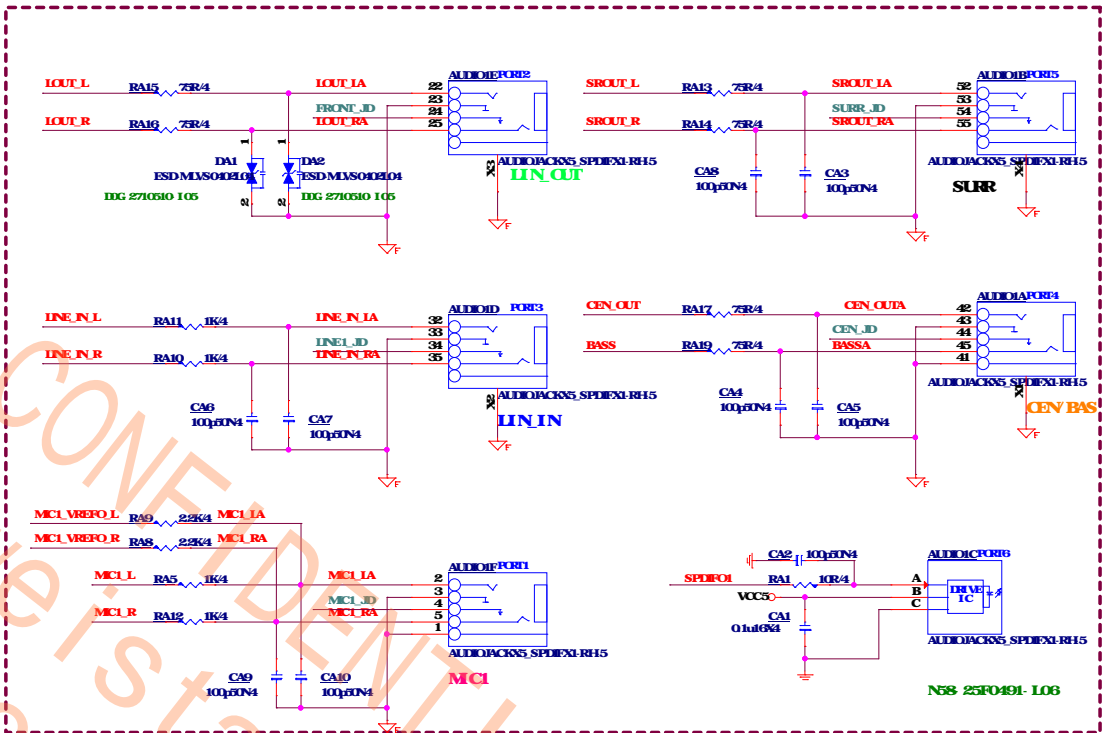
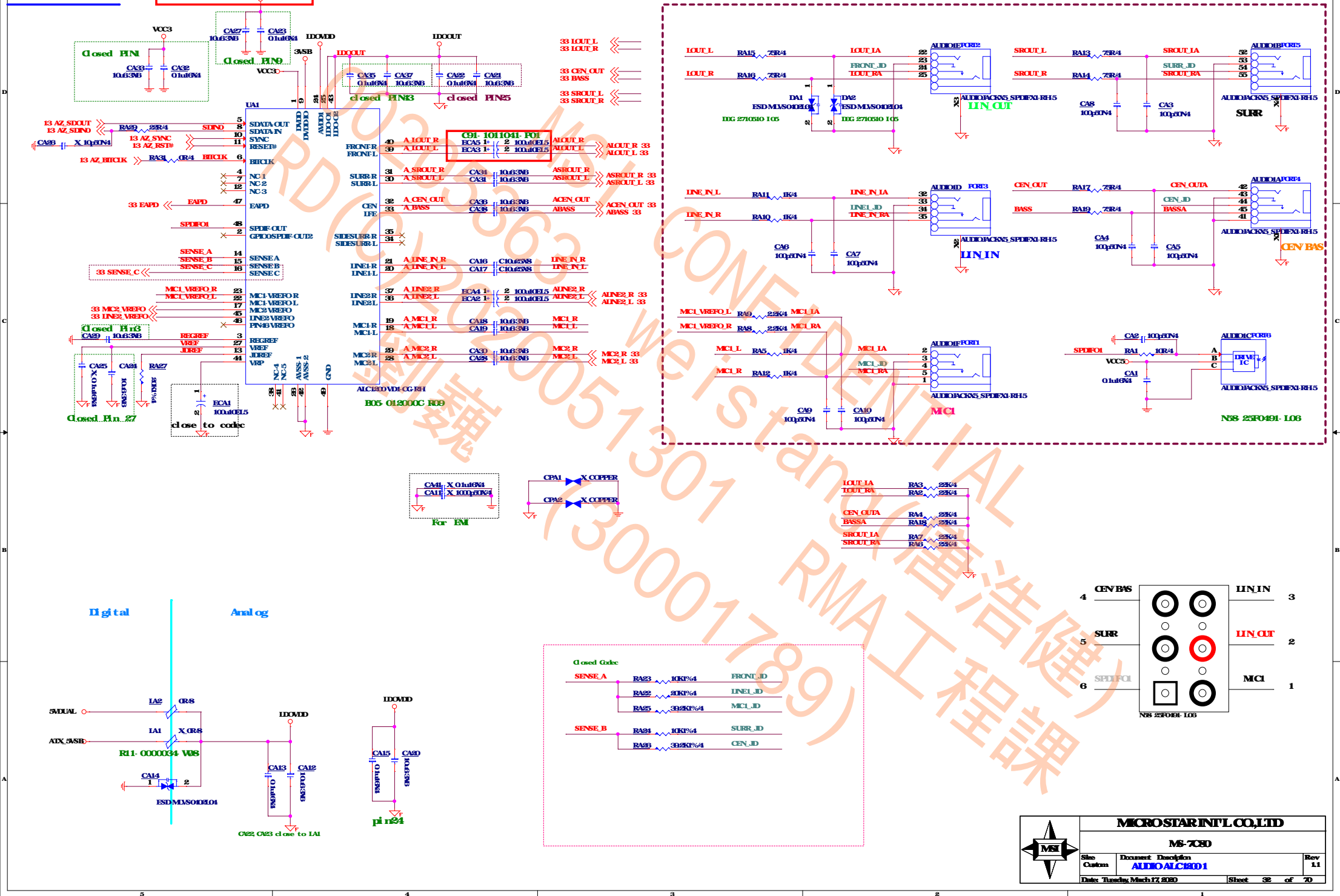
1. Mde GPIO HIGS can switch PWMDC MDE



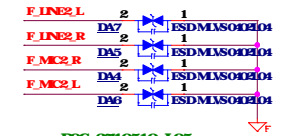
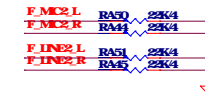
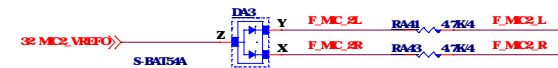
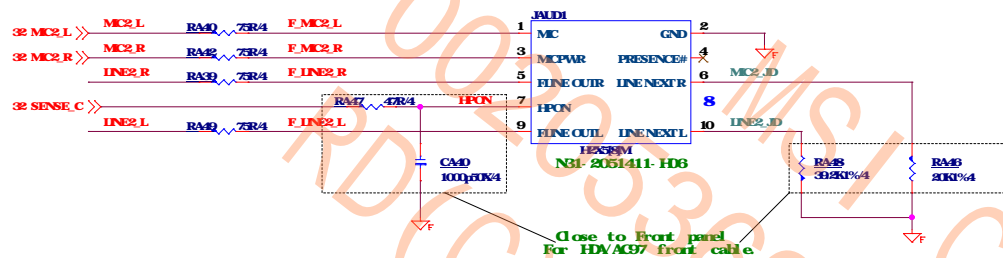
ALC1200

follow PCH power well
need check 3MSB

HN 1~12, 47~49 reference GND
others reference AGND



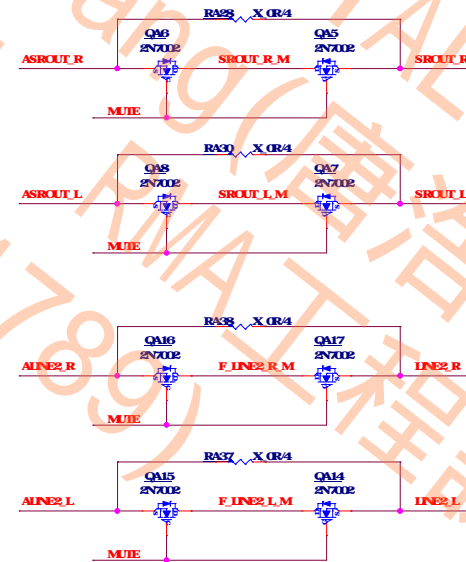
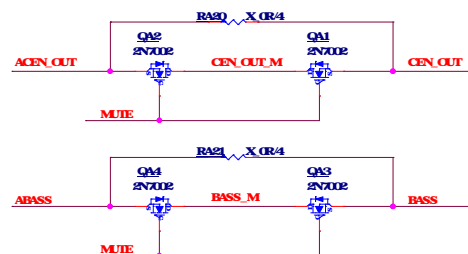
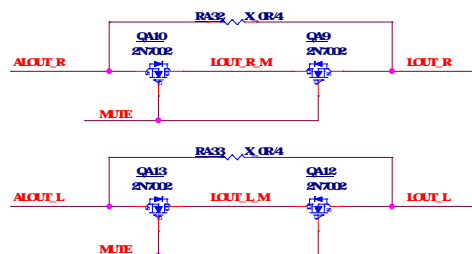
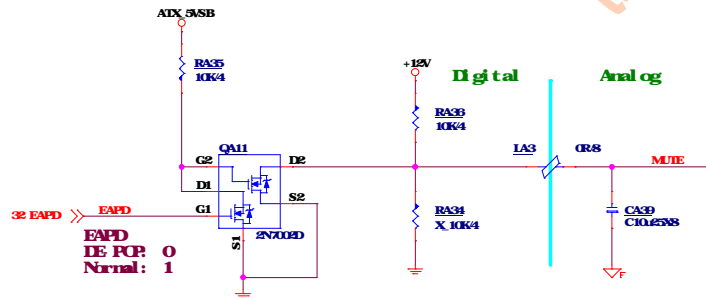
	MICROSTAR INT'L CO., LTD		
	MS-7080		
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DDG 2710510-105
Close to Front panel

ESD protect
DDG 2710510-105
AM: DDG 2850500 SIO

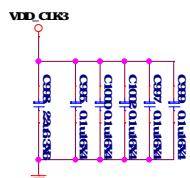
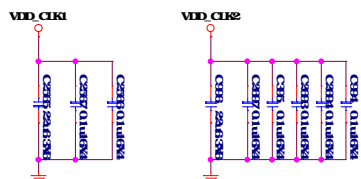
De POP circuit



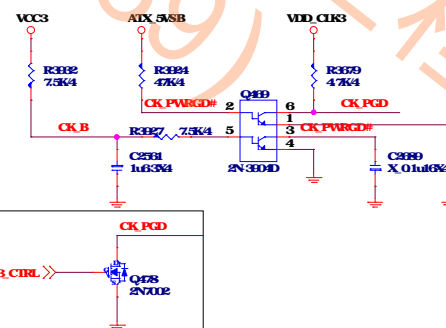
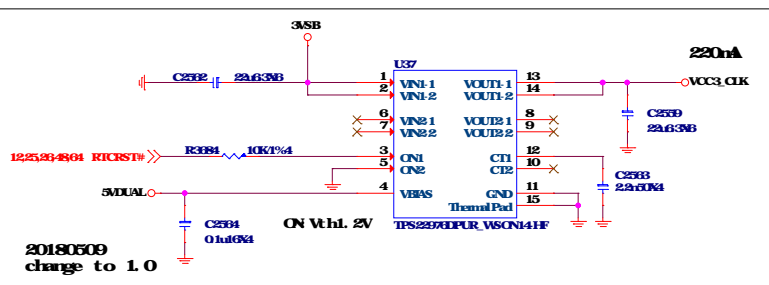
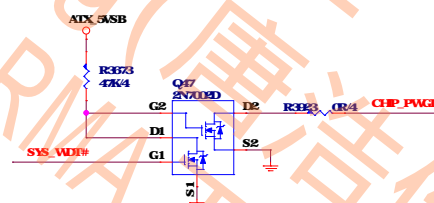
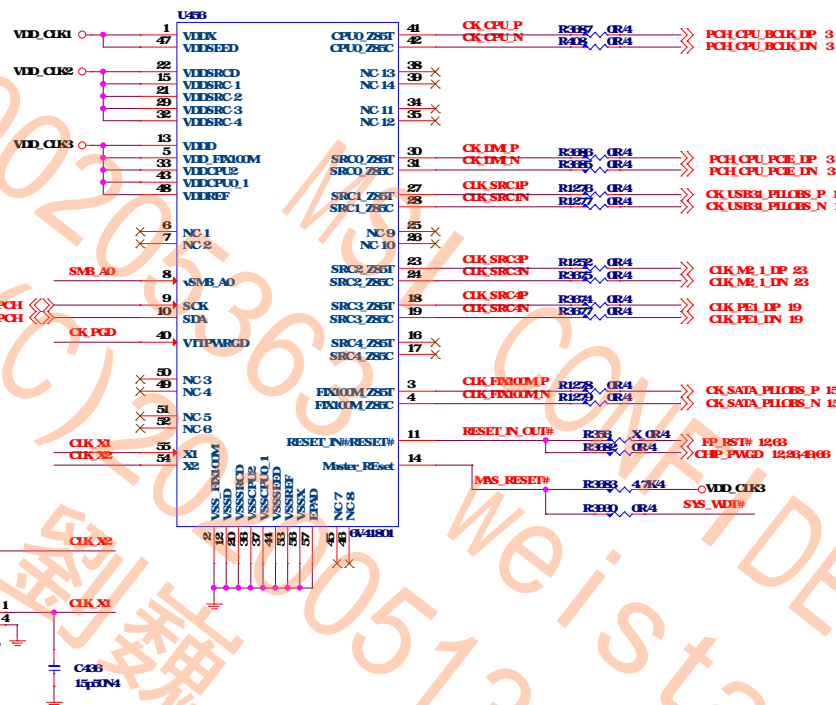
—>> IOUT.L 32
—>> IOUT.R 32
—>> SROUT.L 32
—>> SROUT.R 32
—>> CEN_OUT 32
—>> BASS 32
—>> ASROUT.R 32
—>> ASROUT.L 32
—>> ACEN_OUT 32
—>> ABASS 32
—>> ALINE2.R 32
—>> ALINE2.L 32

MICROSTAR INT'L CO., LTD			
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VCC3_CLK0  **R3881**  **OR6**  **VDD_CLK1**
VCC3_CLK0  **R3881**  **OR6**  **VDD_CLK2**
VCC3_CLK0  **R3880**  **OR6**  **VDD_CLK3**



SMB_A0	ADDR
0	D2/D3
1	D8/D9



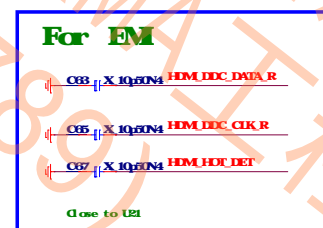
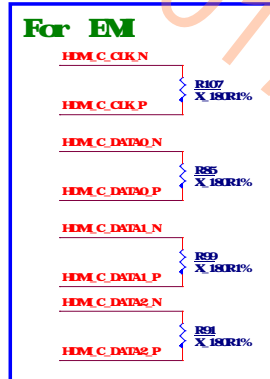
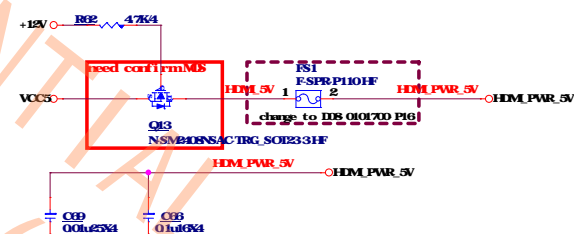
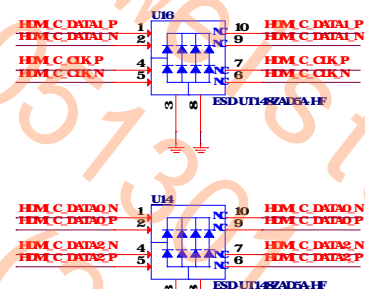
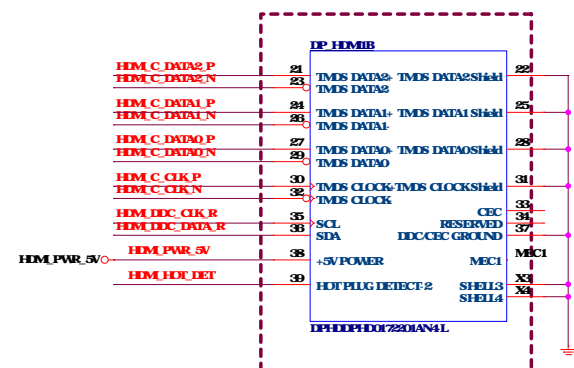
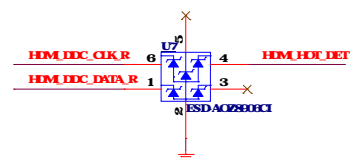
Site Custom	Document Description 019 Clock Gen 6V41892	Rev 1.1
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LAN Connector



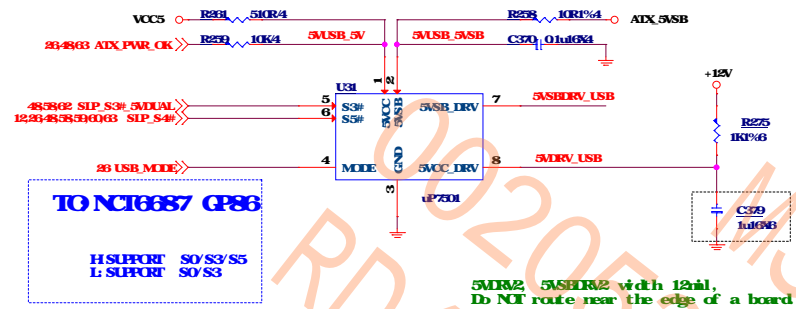
ESD Protect
UL58UL6 close to connector



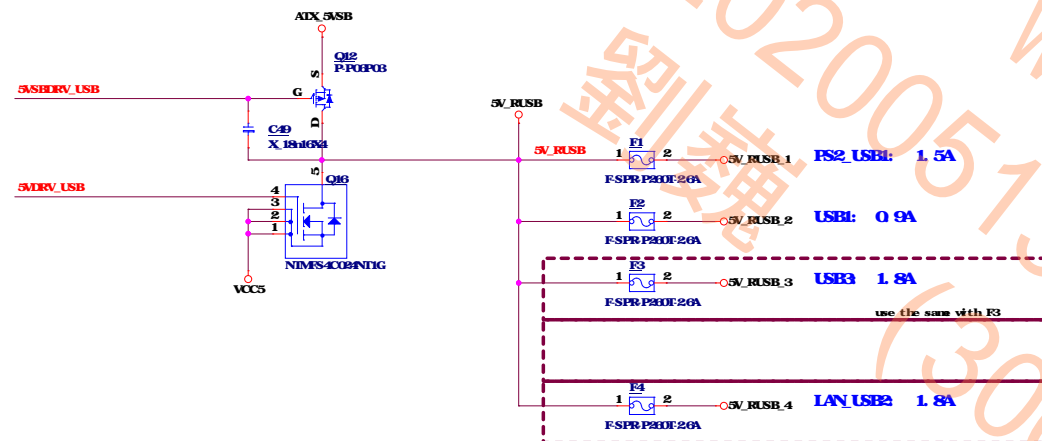




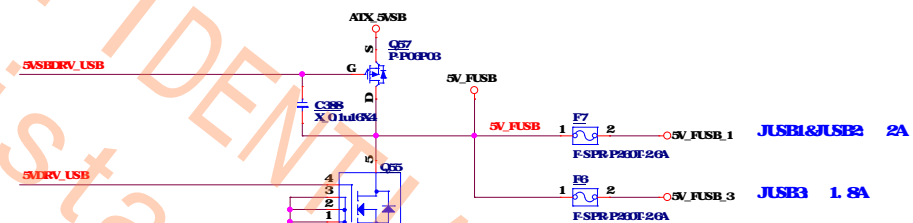
USB Power

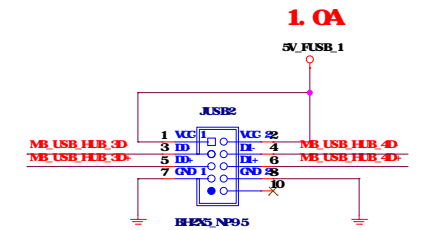


Rear USB Port Power



Front USB Port Power





S3 Wake up (Default)

Bus-Powered 0
Self-Powered 1

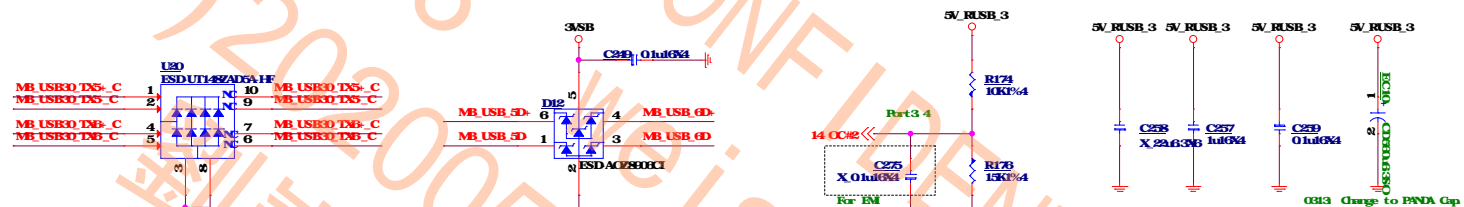
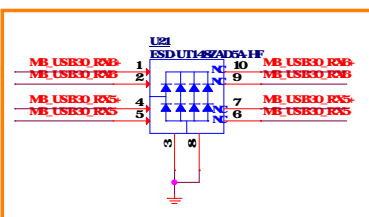
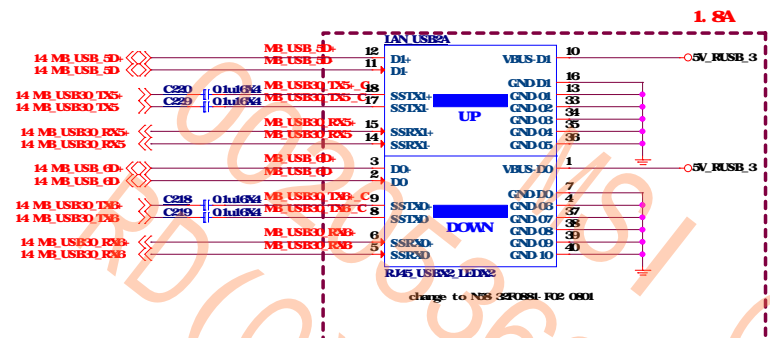
CRB is 680rlna change to 619R
For Met USB Eye Diagram Pass.



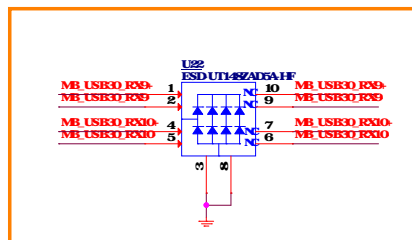
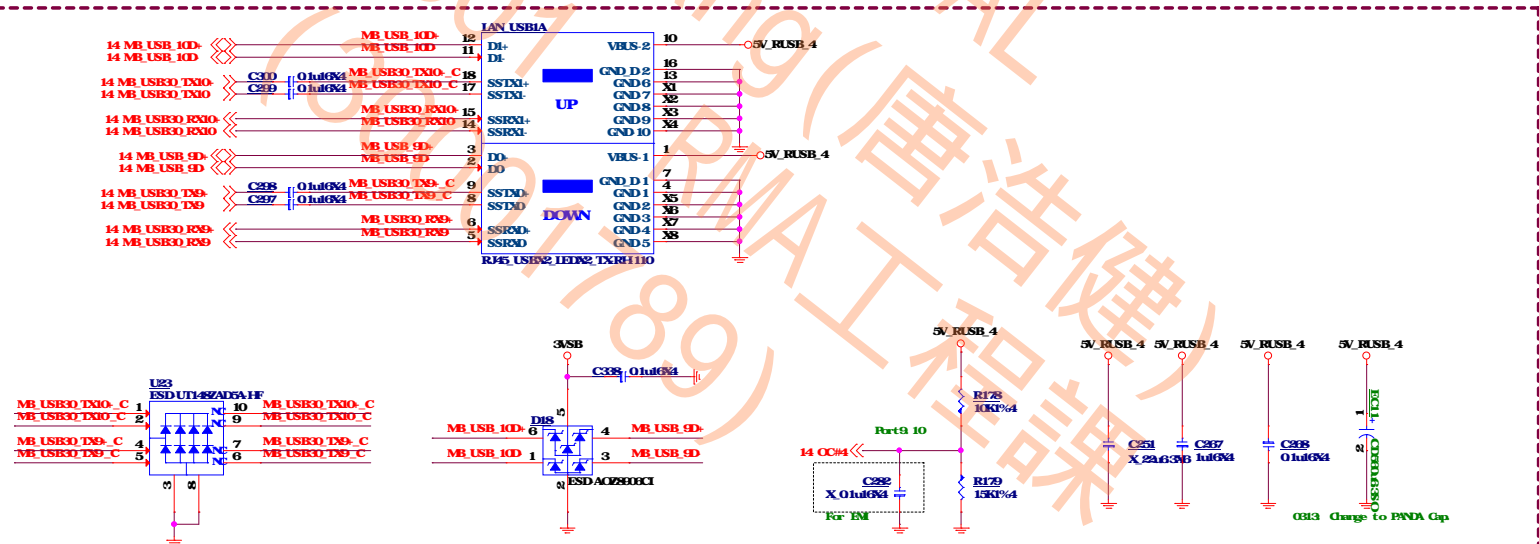
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Rear LAN USB3 1 Gen1



Rear LAN USB3 1 Gen1

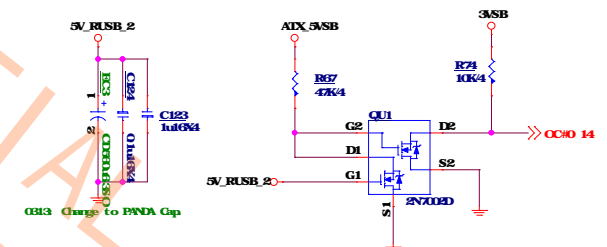
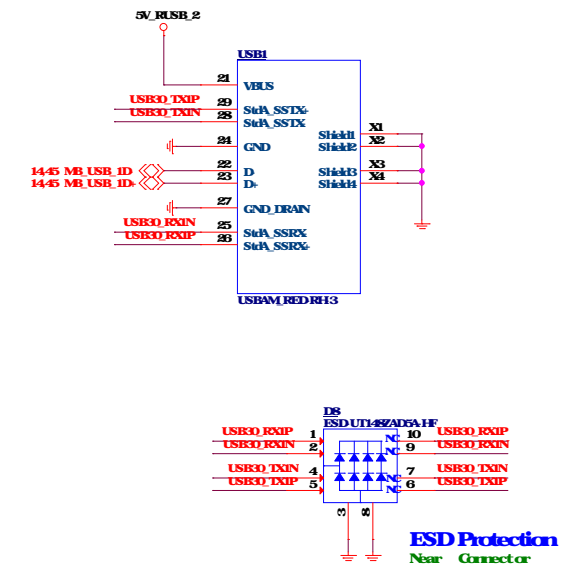


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35B				
R144	4764	UTL_EN		
R139	4764	UTL_ROUTE_EN		
R140	X CR4	UTL_PGA	R142	X R164
R139	X CR4	UTL_PGAS	R133	X OR80R02
R139	X CR4	UTL_PGA	R140	X OR80R02
R139	X CR4	UTL_PGAS	R133	X OR80R02
R147	X CR4	UTL_SVWA	R143	X OR80R02
R131	X CR4	UTL_SVWB	R134	X OR80R02



	HIGH	LOW
EN	Normal operation	Power down mode
RWDET_EN	Receive Enable	Receive Disable

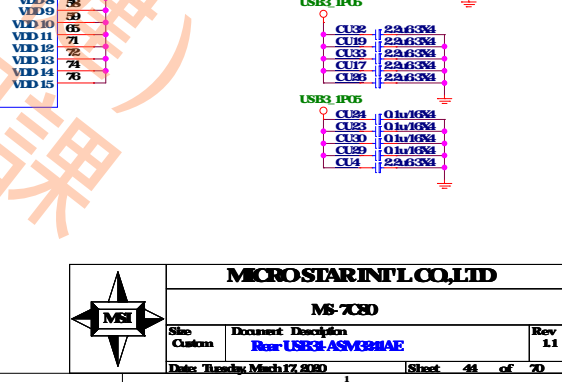
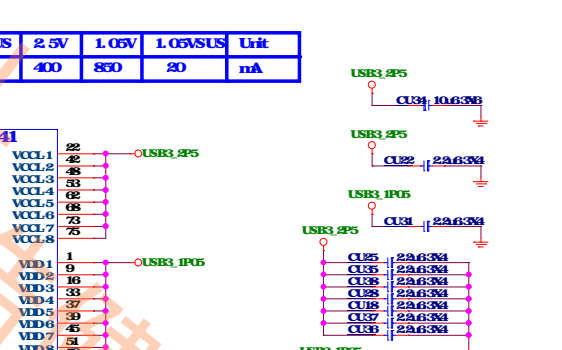
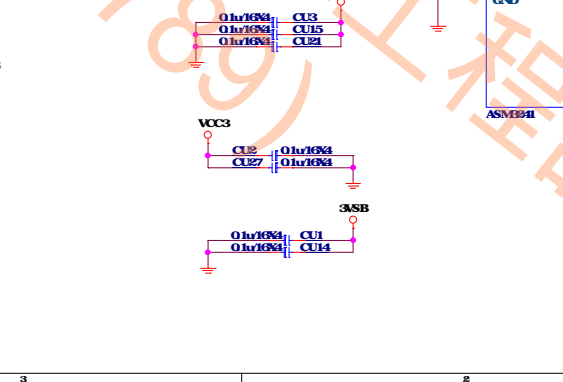
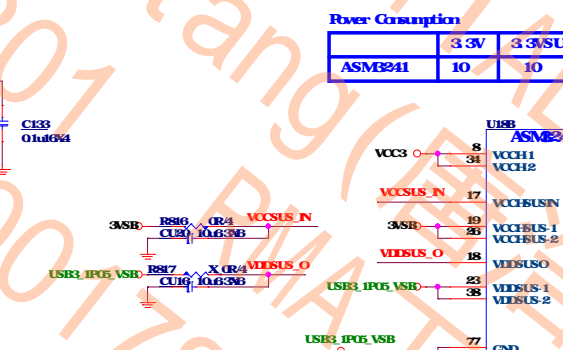
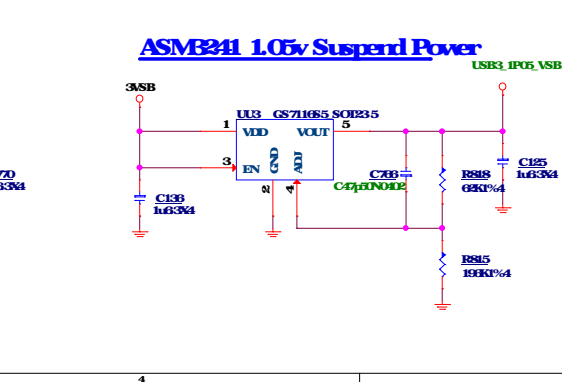
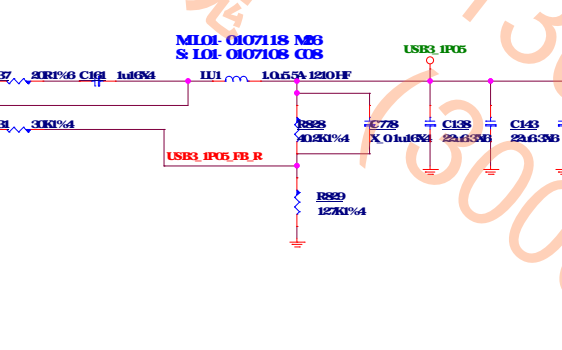
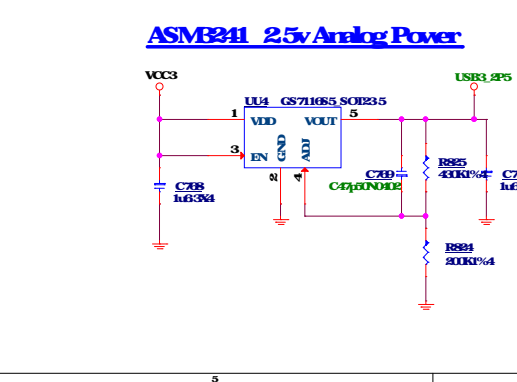
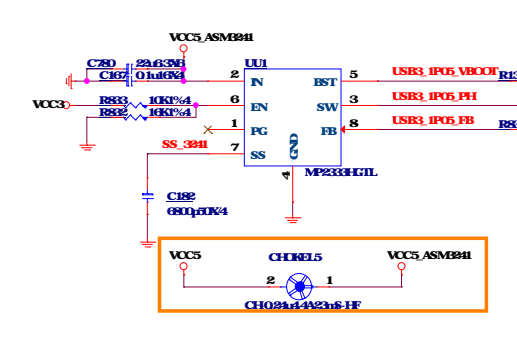
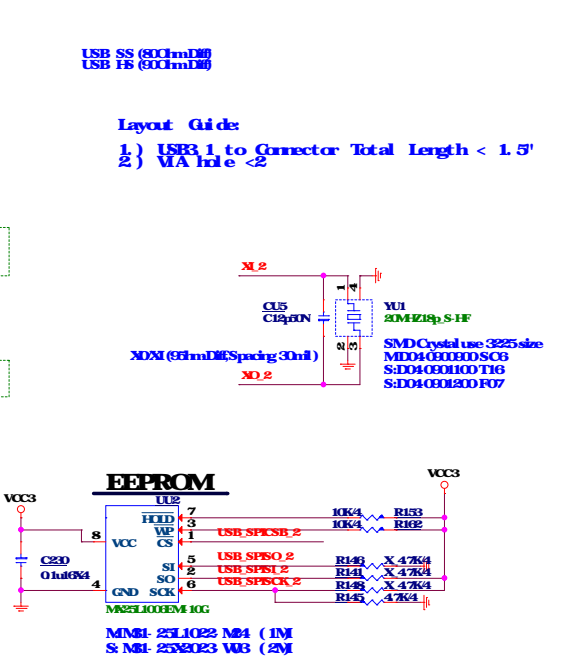
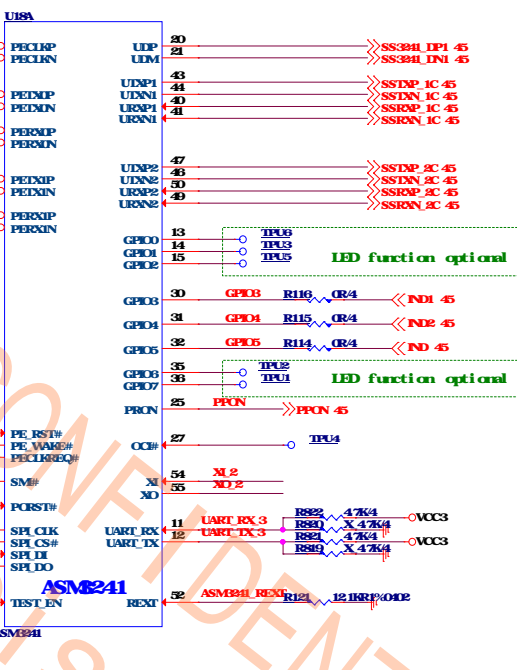
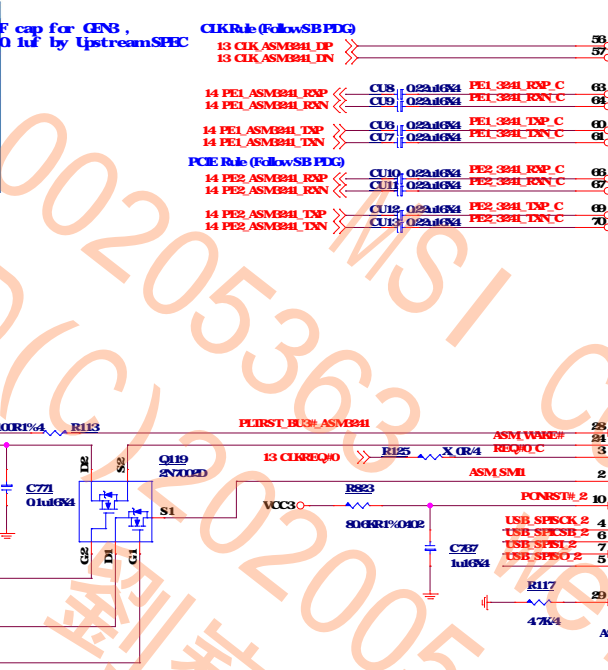
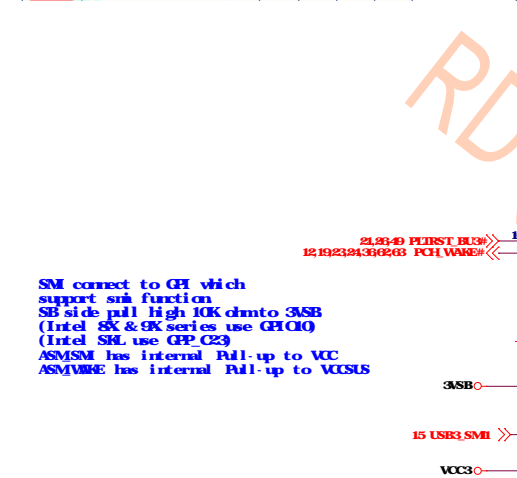
```

UT1_EQA setting Floating , RT15 NC
UT1_EQB setting 65K ohm to GND , RT17 65K ohm
UT1_EGA setting 0 ohm to GND RT11 NC RT12 0 ohm
UT1_EGB setting Floating , RT14 NC
UT1_SVA and UT1_SVB setting Floating RT19 RT21 NC

```

Power On Sequence Timing Specification for Asynchronous mode

Symbols	Parameter	Min	Typ	Max	Unit	Remark
V _{th_pos}	Threshold voltage for PORST# pins	1.38	1.6	1.8	V	
t _{ocr}	OC1# ready after Suspend Power Ready			12	ms	Use 0.22µF cap for GEN3, Gen2 use 0.1µF by UpstreamSPEC
t _{vsr}	Rising time for Suspend and normal Power Ready			10	ms	
t _{norm}	Timing for all normal Power Ready	50			ms	Note 1
PORST1	Timing for all normal Power Ready to Power On Reset (when suspend power domains are existed)	10		80	ms	
	Timing for all normal Power Ready to Power On Reset (when suspend powers connect to normal power directly)	60		80	ms	



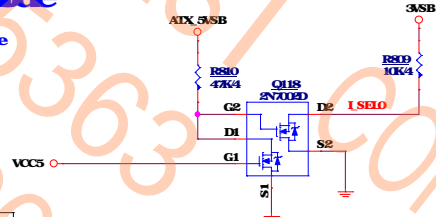
Current Mode

3A under S0 mode
1.5A under S3 mode

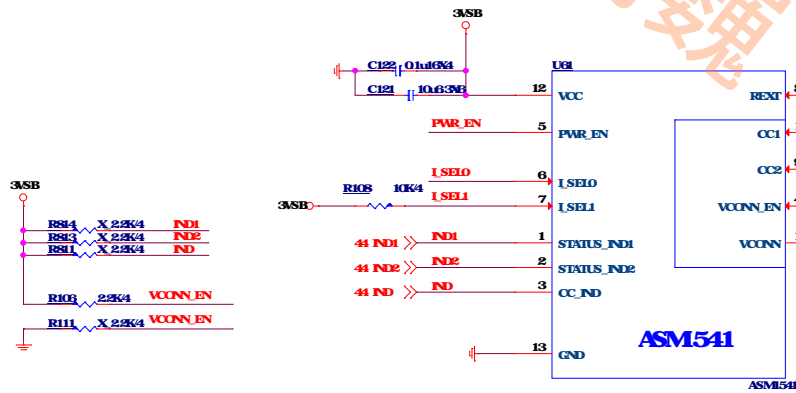
I_{SENSE}: I_{SENSE1}

X 0	Default for 900mA
0 1	1.5A@5V
1 1	3A@5V

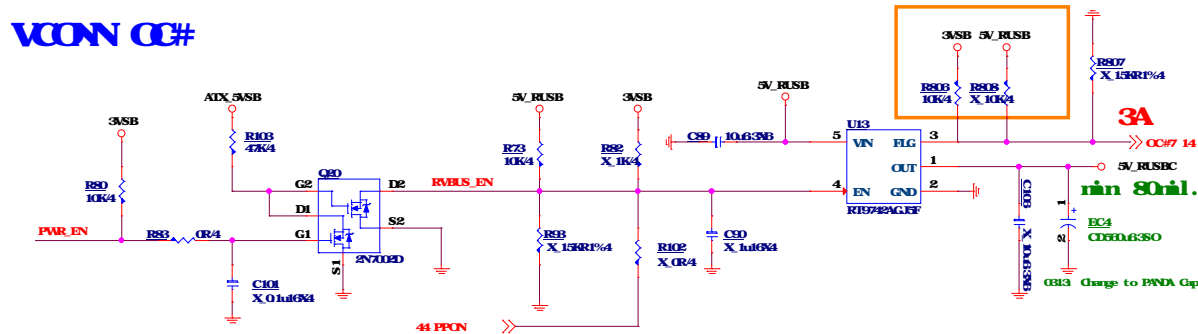
1.5A under S3 mode
3A under S0 mode



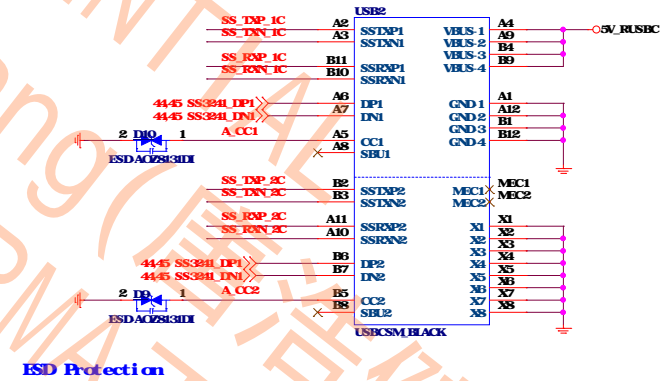
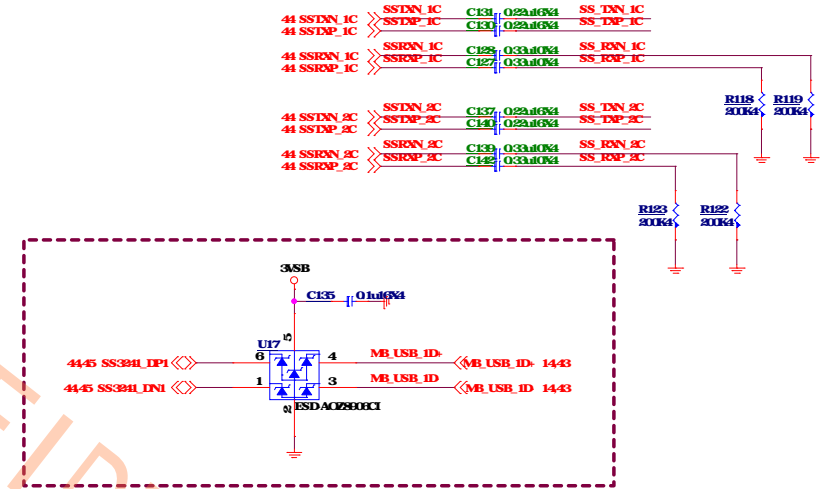
USB 3.2 Type C



VCONN CC#



TYPE C

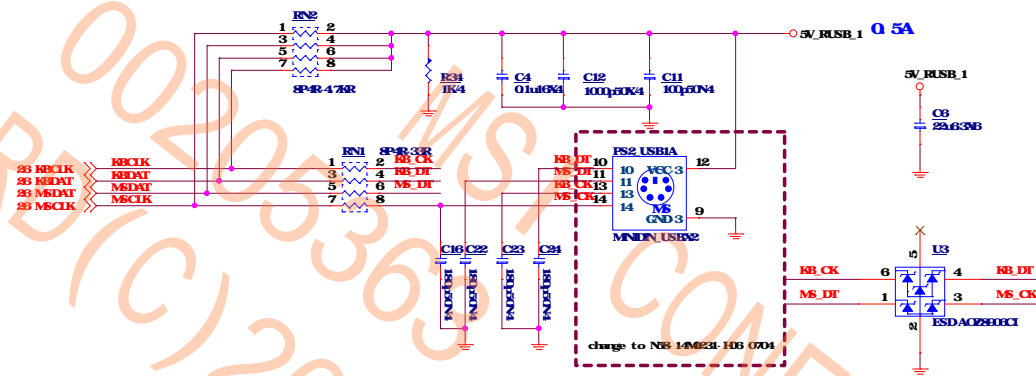


ESD Protection

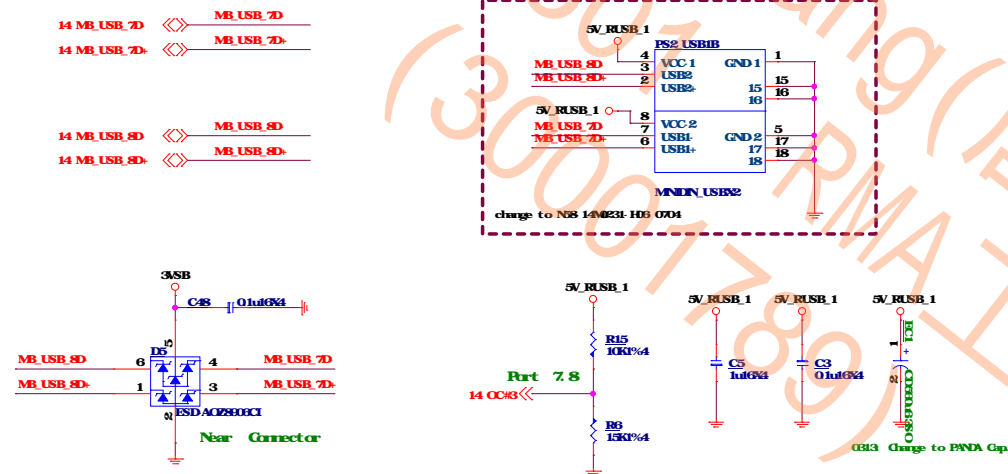


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PS2 Keyboard & Mouse Connector



PS2 USB2 0



MICROSTAR INT'L CO., LTD

MS-7080

	Size
	Custom

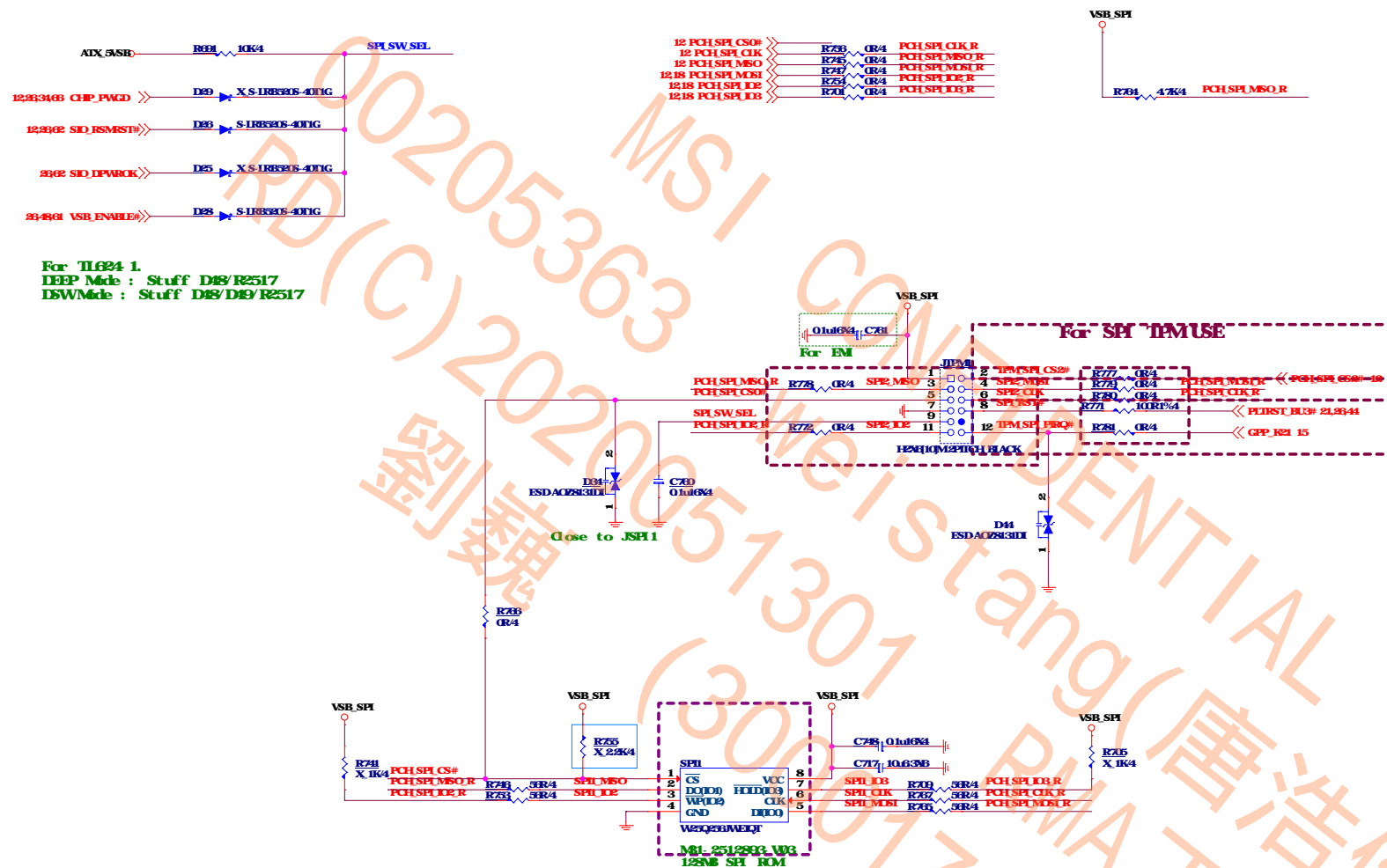
Document Description
PS2 USB1

Rev
11

Date: Tuesday, March 17, 2020

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For TL624 1.
DEEP Mode : Stuff D18/R2517
DSWMode : Stuff D18/D19/R2517



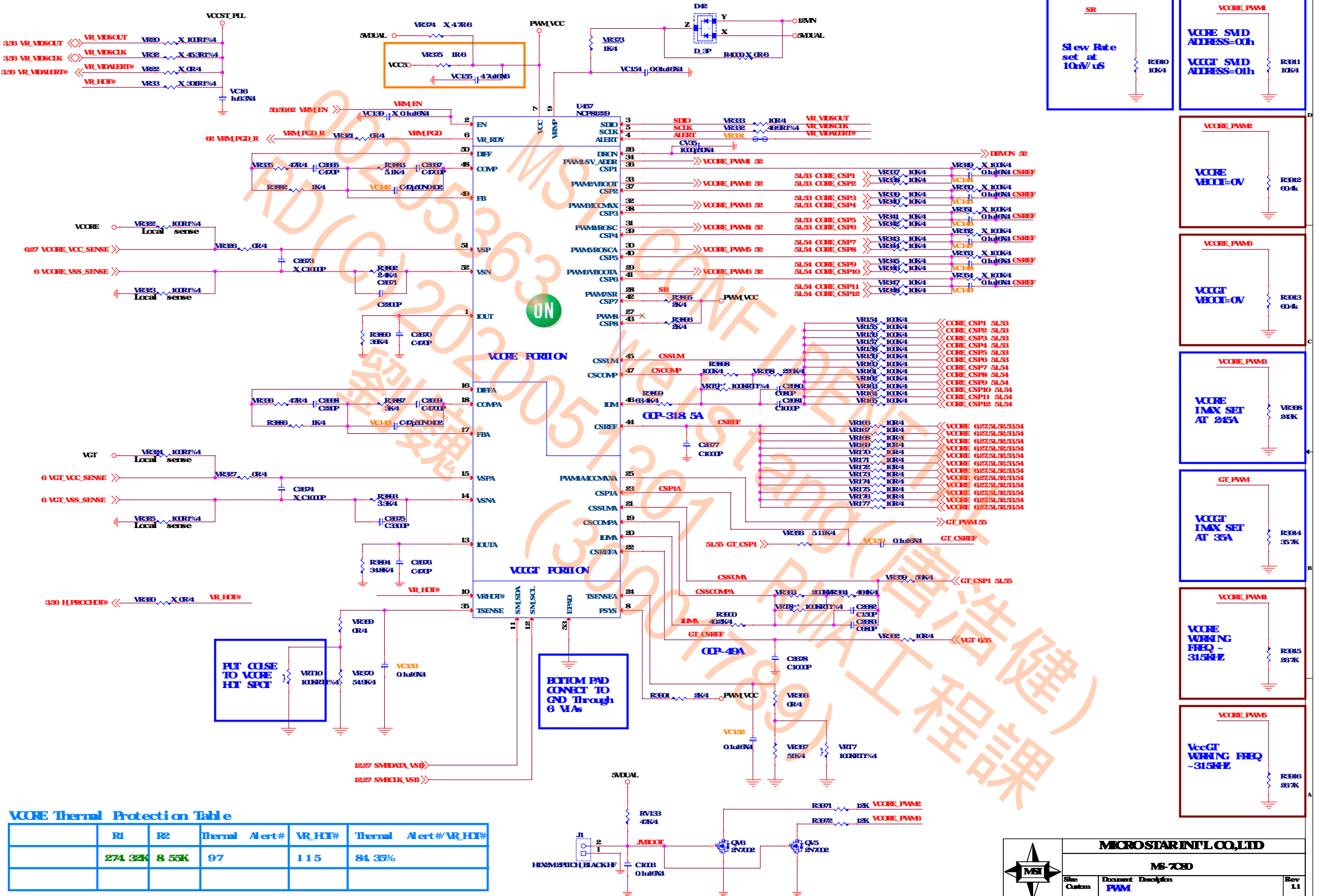
MS-7080

	Rev 1.1
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Date: Tuesday, March 12, 2020

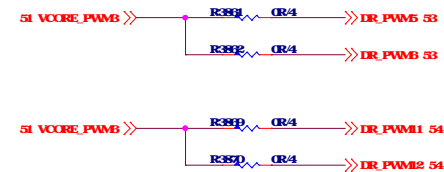
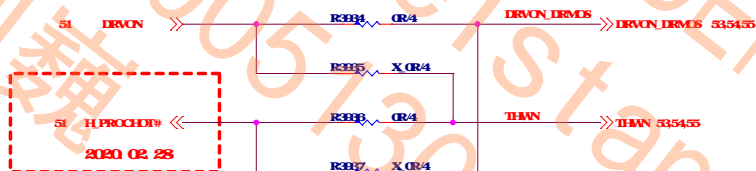
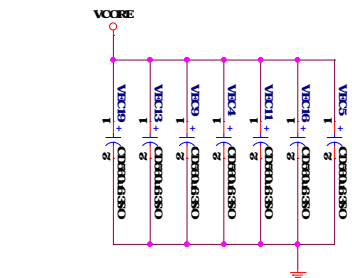
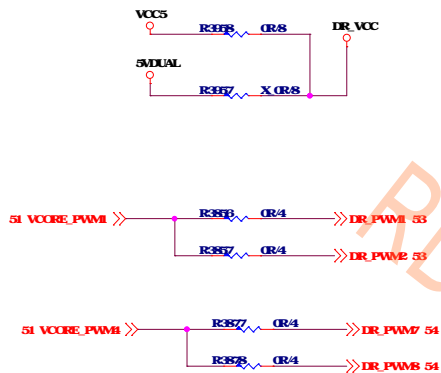
Date: Tuesday, March 17, 2020		Sheet 49 of 70
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NAME(S)	ADDRESS	APPROX. DATE	TYPE	NO.	OR	PL
1						

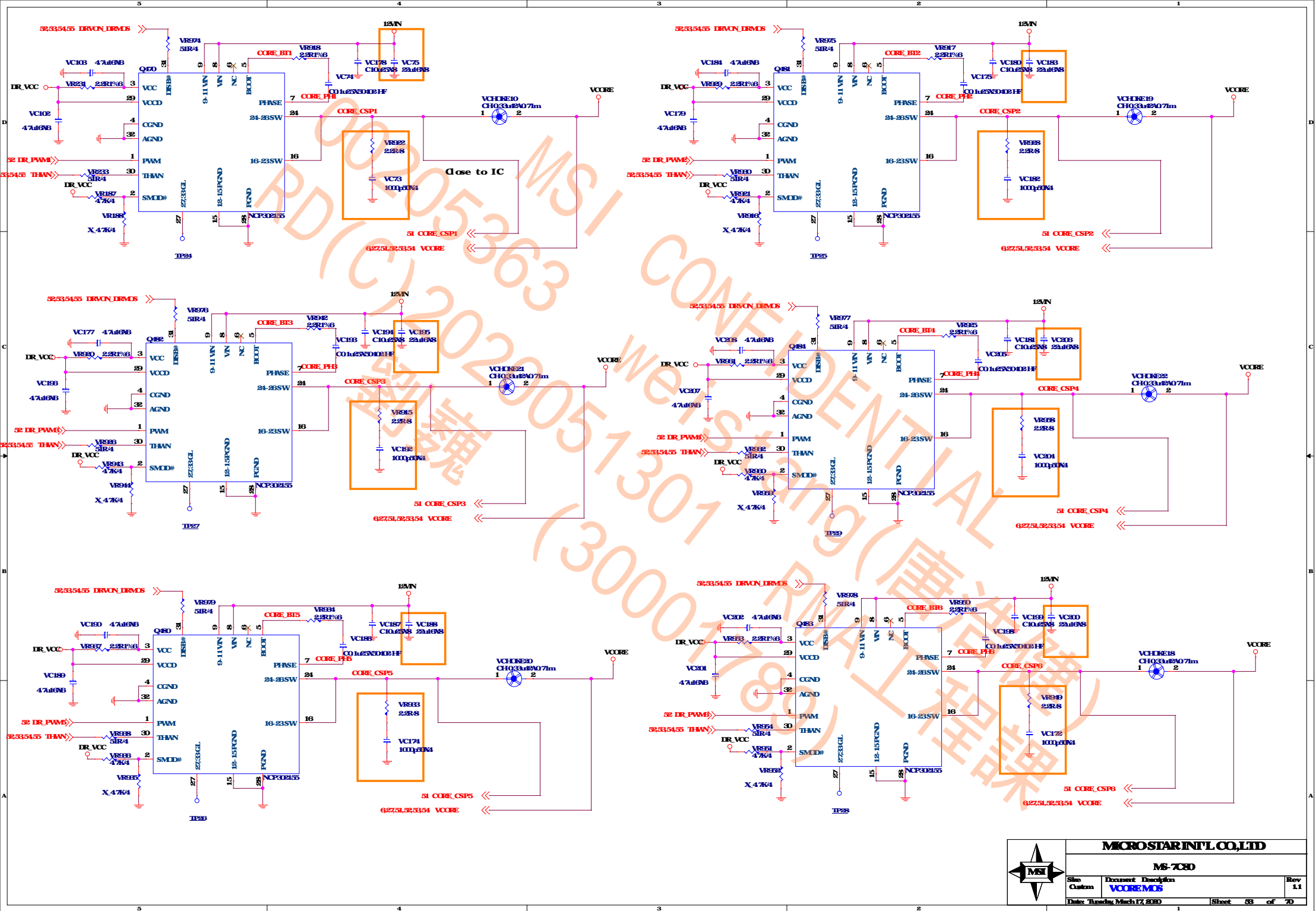


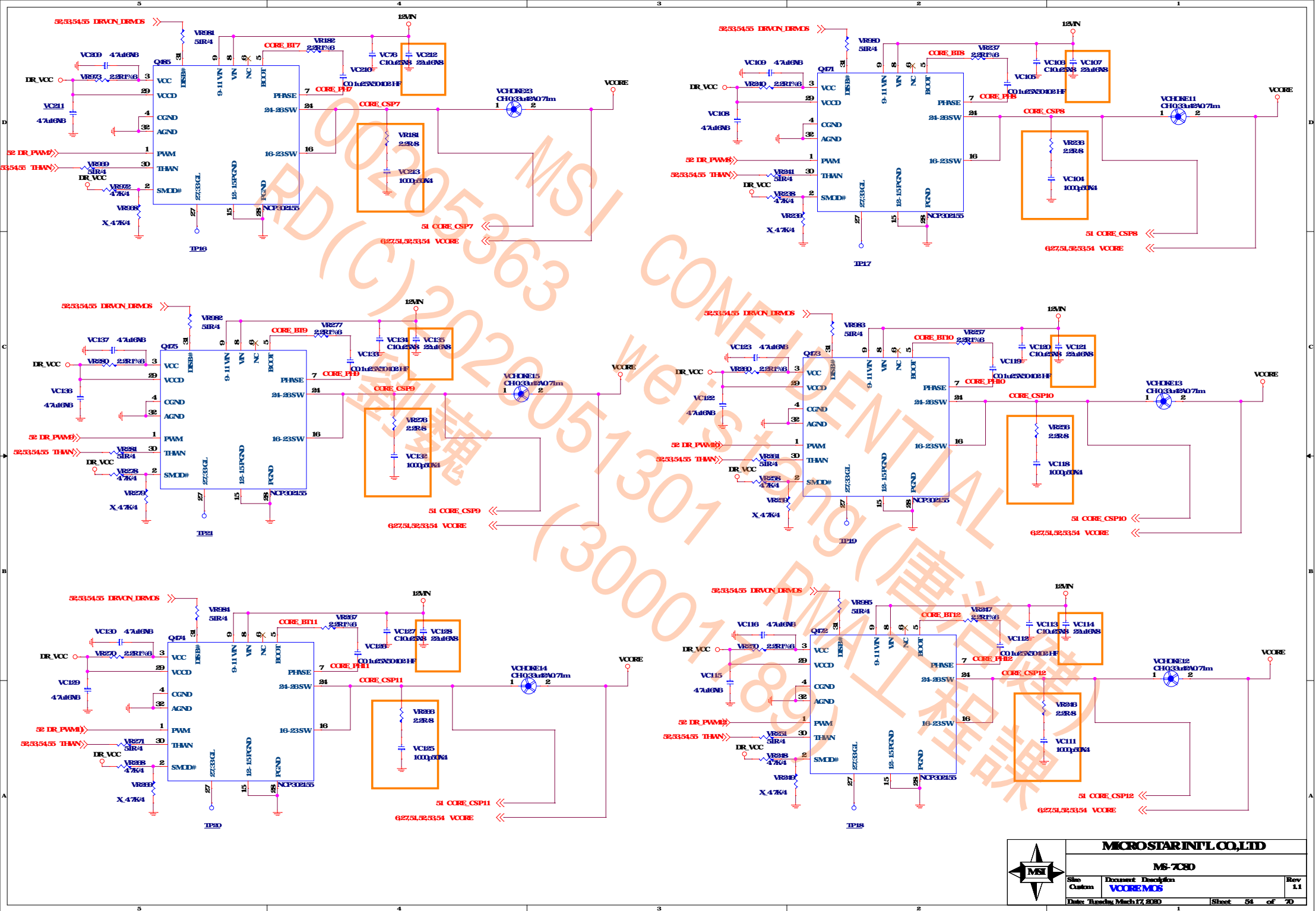
Vcore Thermal Protection Table

	R1	R2	Thermal Alert#	VR_HOI#	Thermal Alert#	VR_HOI#
	274 32K	8 55K	97	1 15	84 35%	

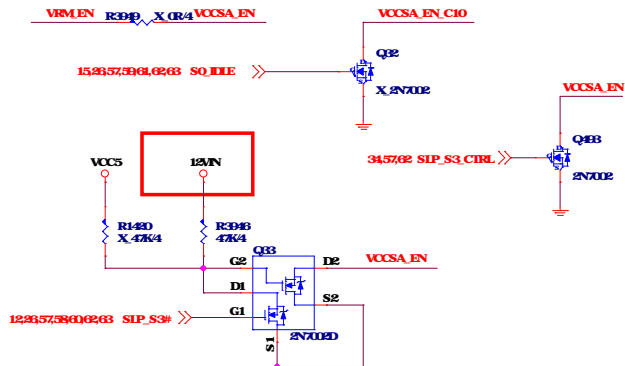
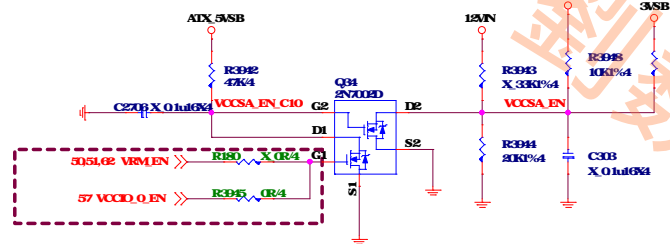
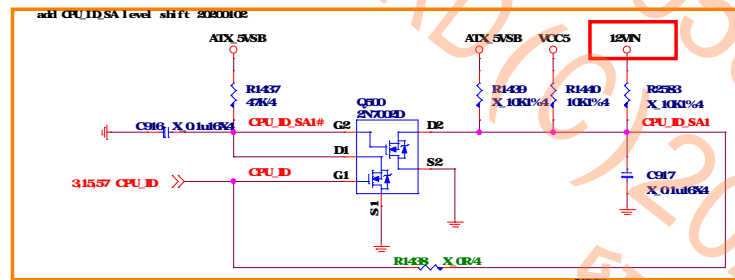


VCC6 << VCC6 62751.3354

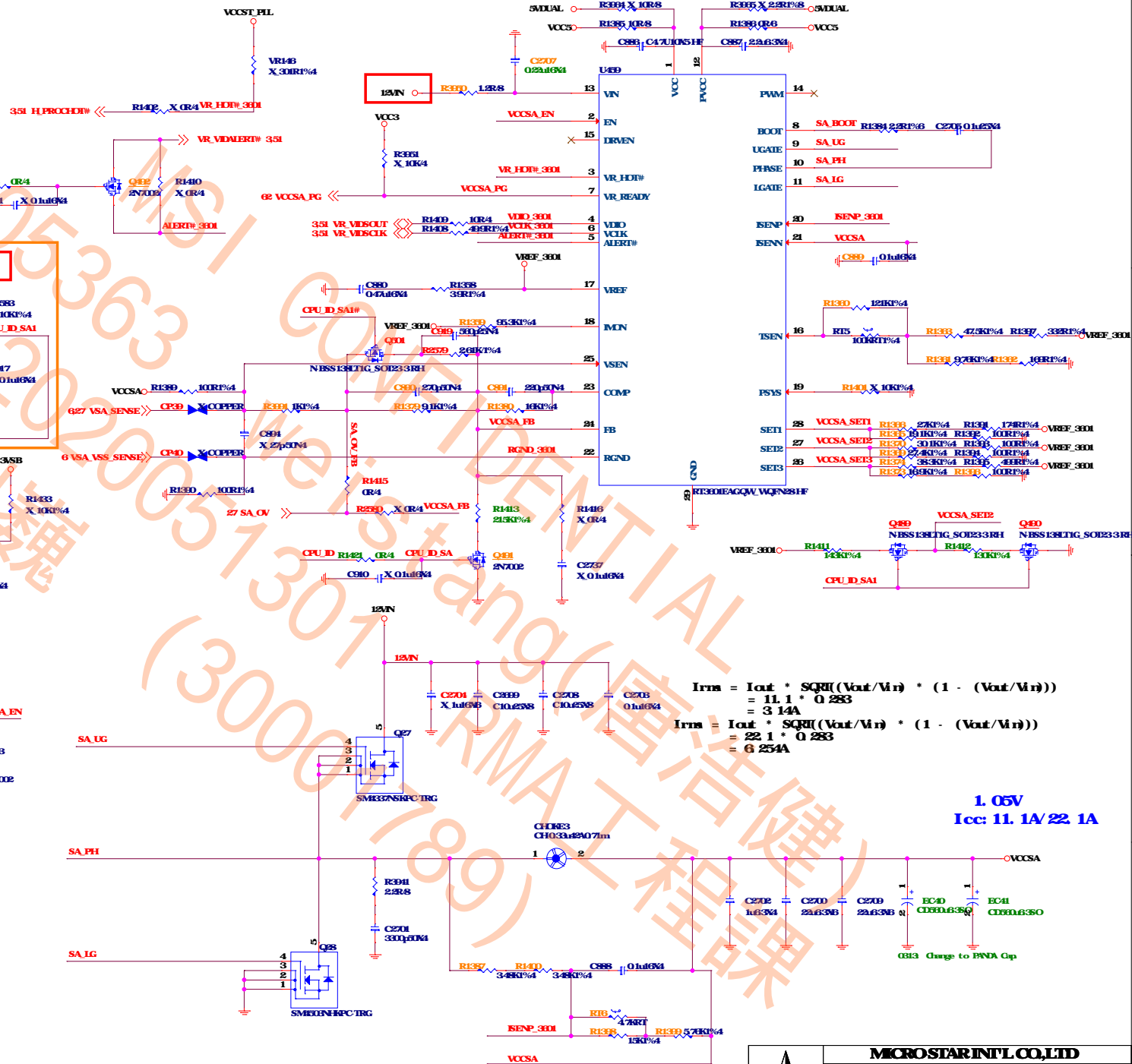




SA Power: 1.05V, 11.1A/22.1A



SLP_S3# assertion to VC, VCC5, VCCIO and VCCSA rails completely off.
SLP_S3# assertion to VR disabled max lus



$$I_{rms} = I_{out} \cdot \sqrt{((V_{out}/V_{in}) \cdot (1 - (V_{out}/V_{in})))}$$

$$= 11.1 \cdot 0.283$$

$$= 3.14A$$

$$I_{rms} = I_{out} \cdot \sqrt{((V_{out}/V_{in}) \cdot (1 - (V_{out}/V_{in})))}$$

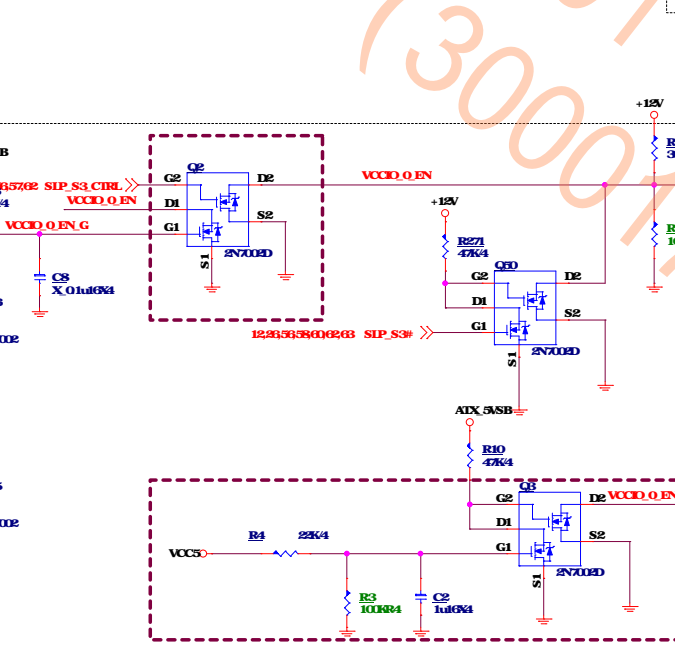
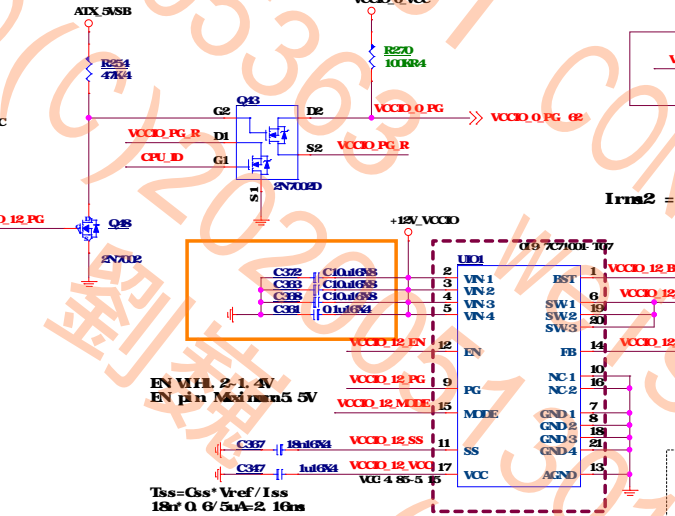
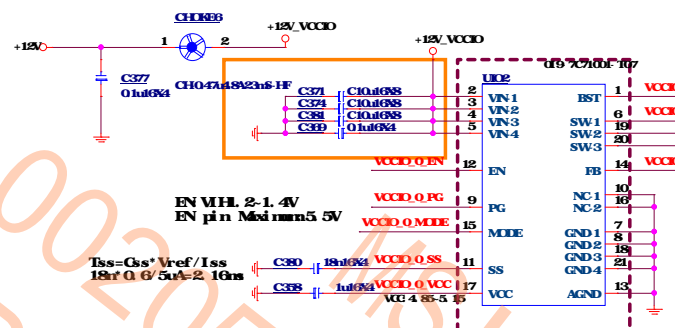
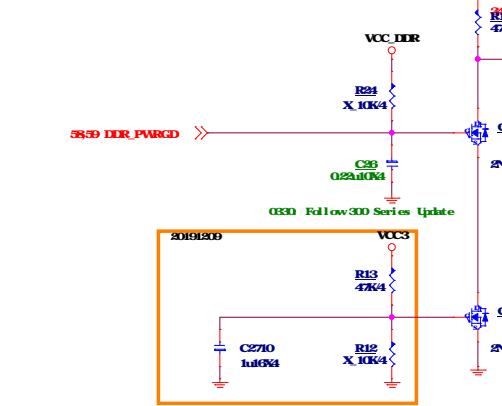
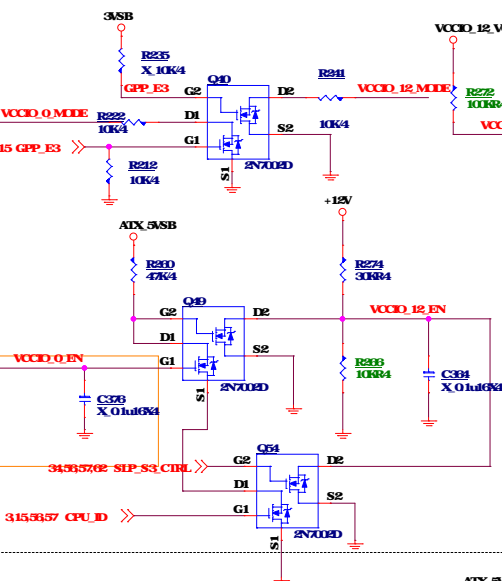
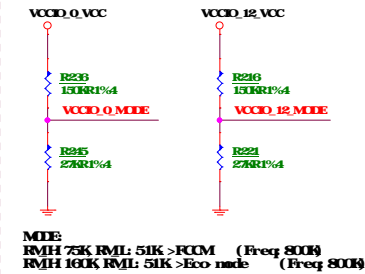
$$= 22.1 \cdot 0.283$$

$$= 6.254A$$

1.05V
Icc: 11.1A/22.1A

VCCIO Power

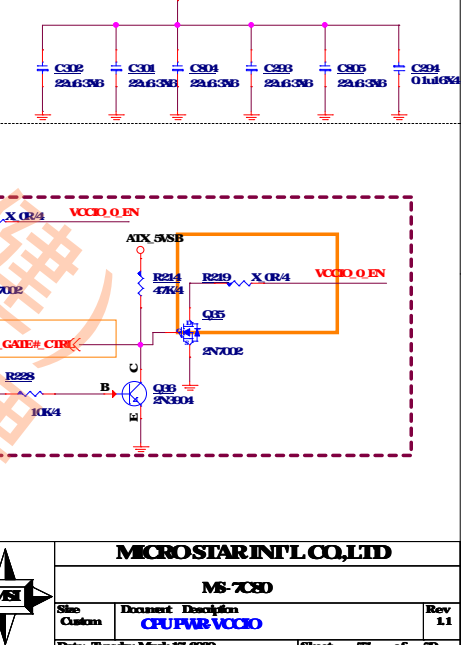
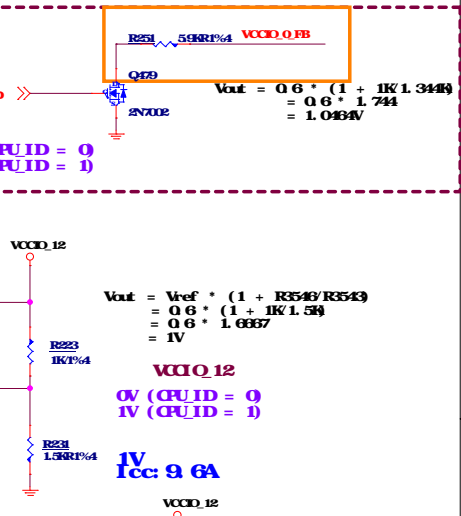
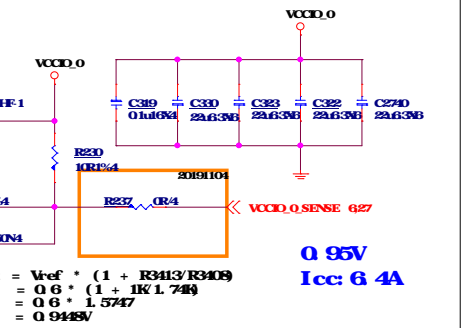
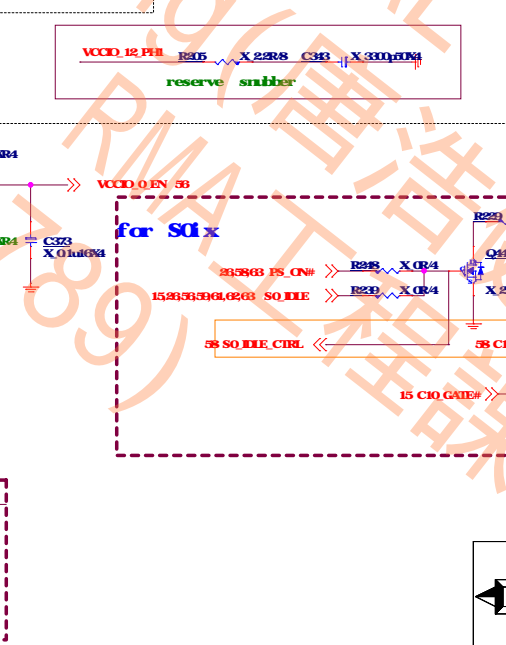
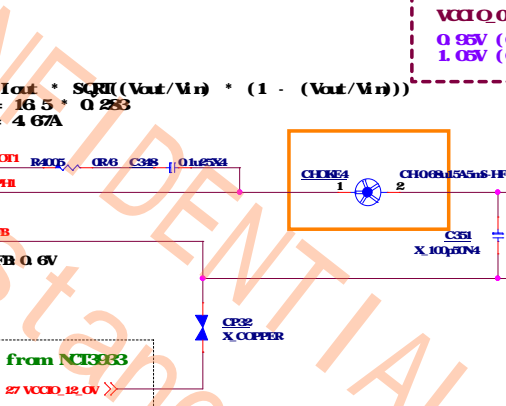
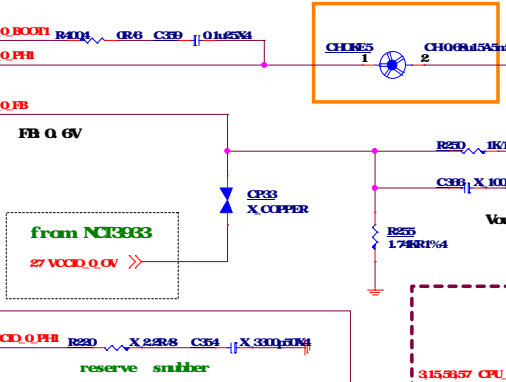
0.95V Icc: 6.4A
1.05V Icc: 16.5A



$$I_{rms1} = I_{out} * \sqrt{SQRT((V_{out}/V_{in}) * (1 - (V_{out}/V_{in})))}$$

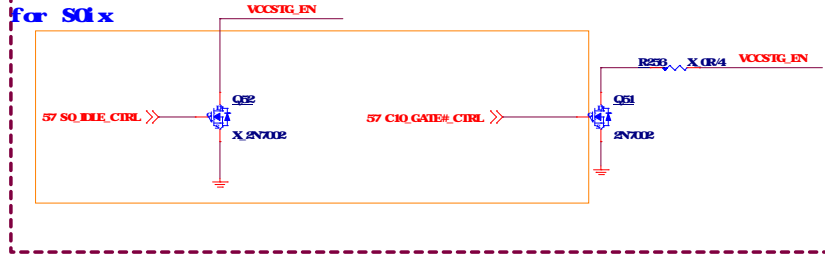
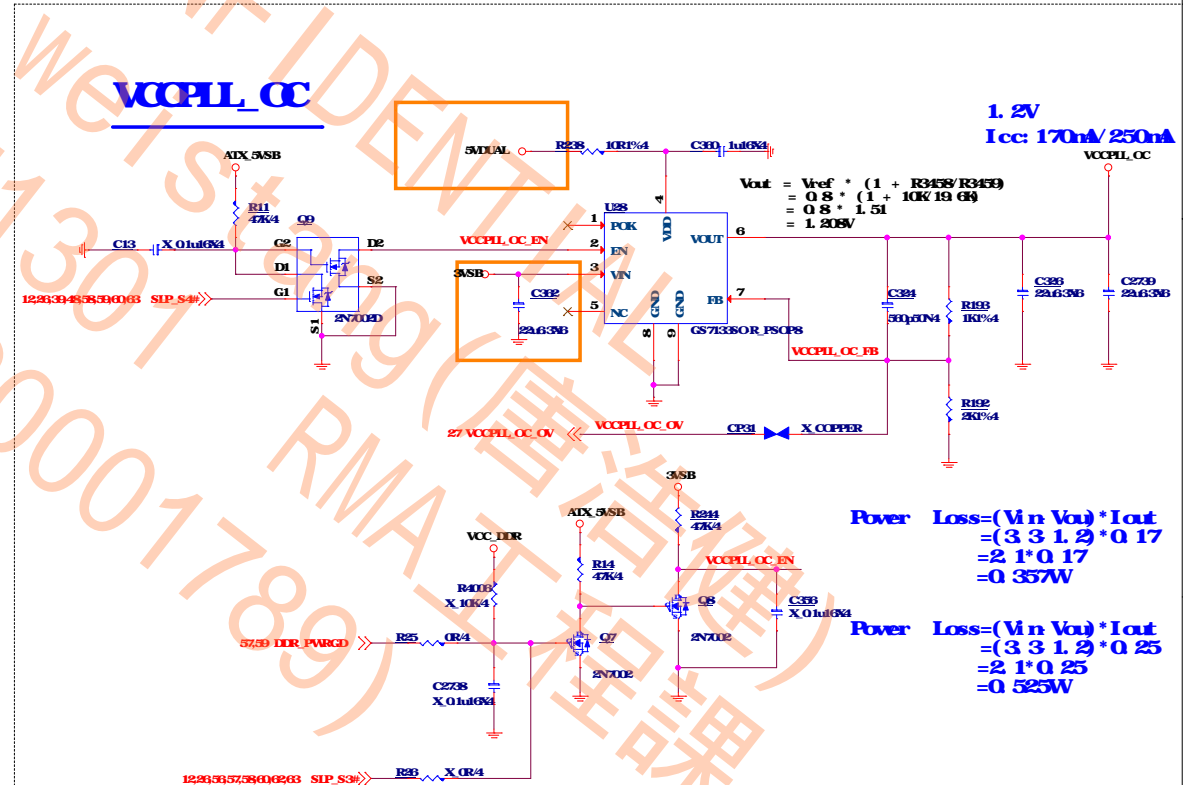
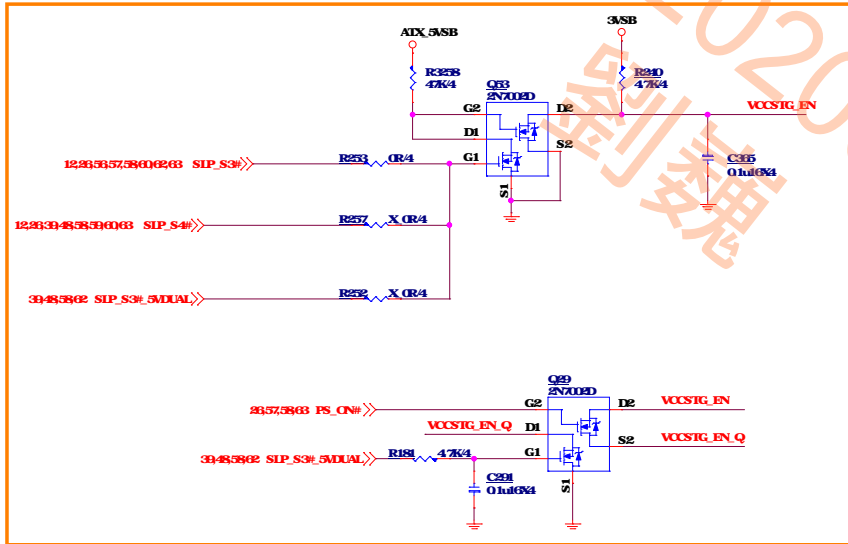
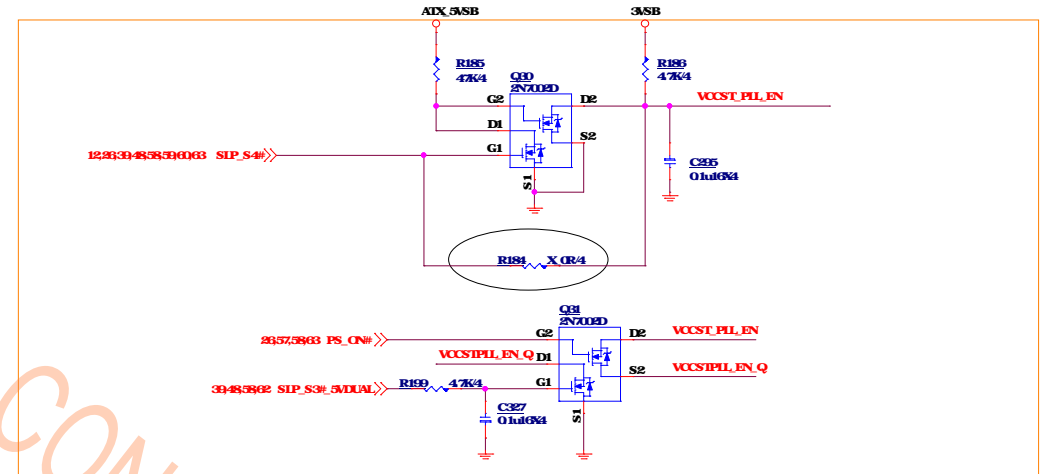
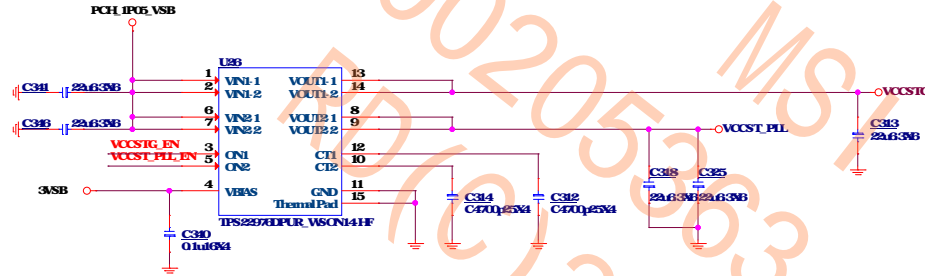
$$= 6.4 * 0.27$$

$$= 1.728A$$



VCCST_PLL 1.05V; 1.15V/2.53A
VCCSIG 1.05V; 0.2A/0.9A

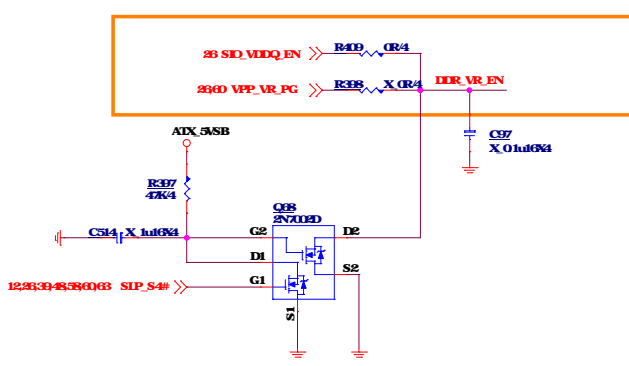
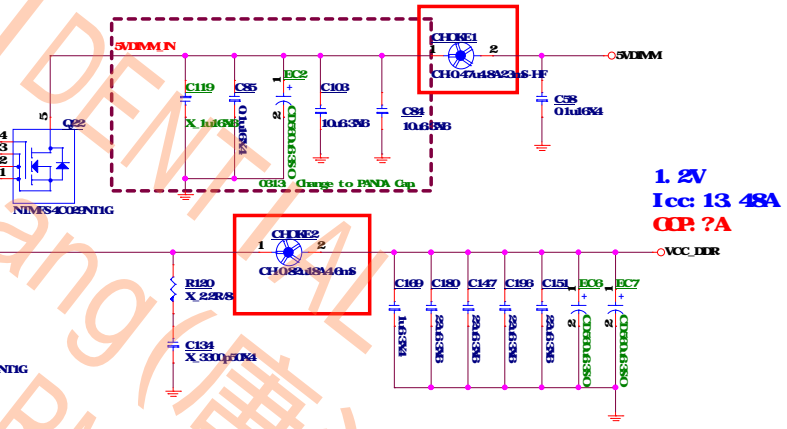
$$\begin{aligned} \text{Power Loss1} &= (I^2) \cdot R_{ds(on)} \\ &= (2.53 \cdot 2.53) \cdot 0.022 \\ &= 6.4 \cdot 0.022 \\ &= 0.141W \\ \text{Power Loss2} &= (I^2) \cdot R_{ds(on)} \\ &= (0.9 \cdot 0.9) \cdot 0.022 \\ &= 0.81 \cdot 0.022 \\ &= 0.018W \end{aligned}$$



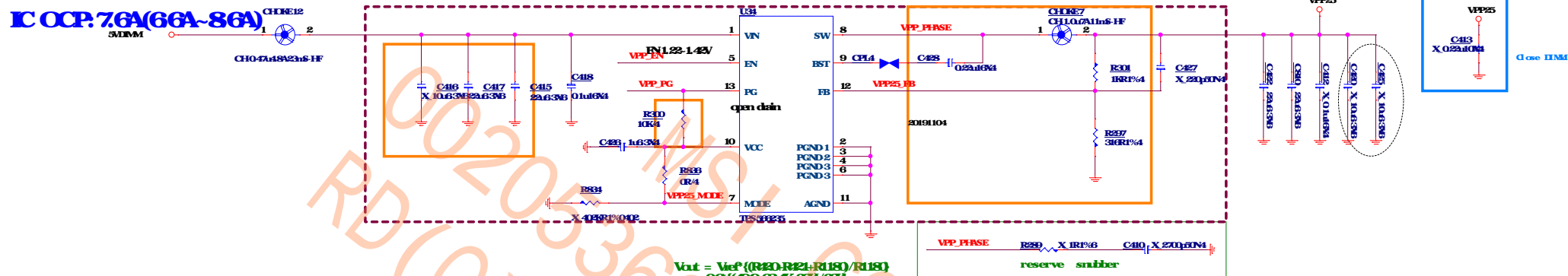
3 68A For CPU
9 1A For 4DIMM
0 7A For DDR VTT

$$\begin{aligned} I_{ocp} &= R_{ocset} \cdot I_{ocset} / R_{iscr}(low) \\ &= 7.5K \cdot 10uA / 3.3m \\ &= 19.23A \\ I_{ocp} &= R_{ocset} \cdot I_{ocset} / R_{iscr}(max) \\ &= 7.5K \cdot 10uA / 4m \\ &= 14.7A \end{aligned}$$

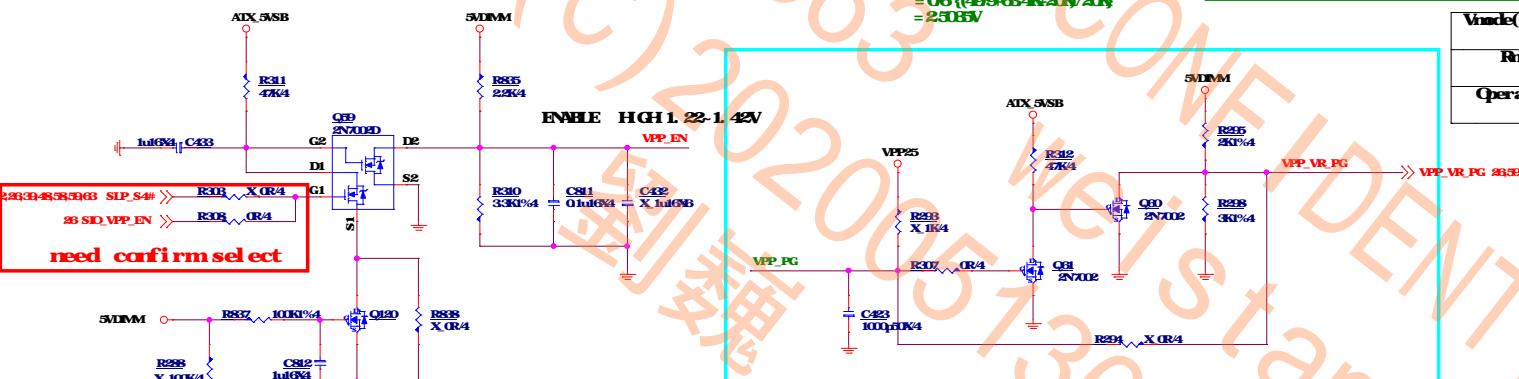
Rdson(Low Si de) 5V
IDB 4002403 005 3 3



IC OCP: 7.6A(66A~86A)

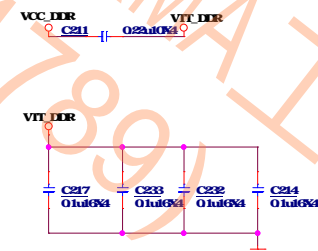
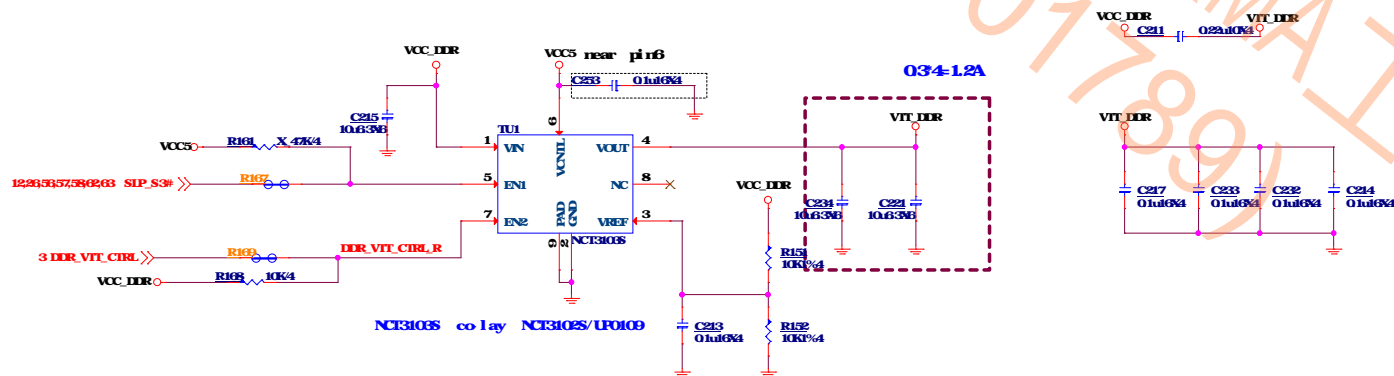


Vmode(VPP25_MDE)	0-0.3V	0.3-1.2V	>1.2V
Rmode	OR	100K-150K	To VCC(recommend) or R-400K
Operating Mode	Eco Mode	On - CF - Audio	ROOM



DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

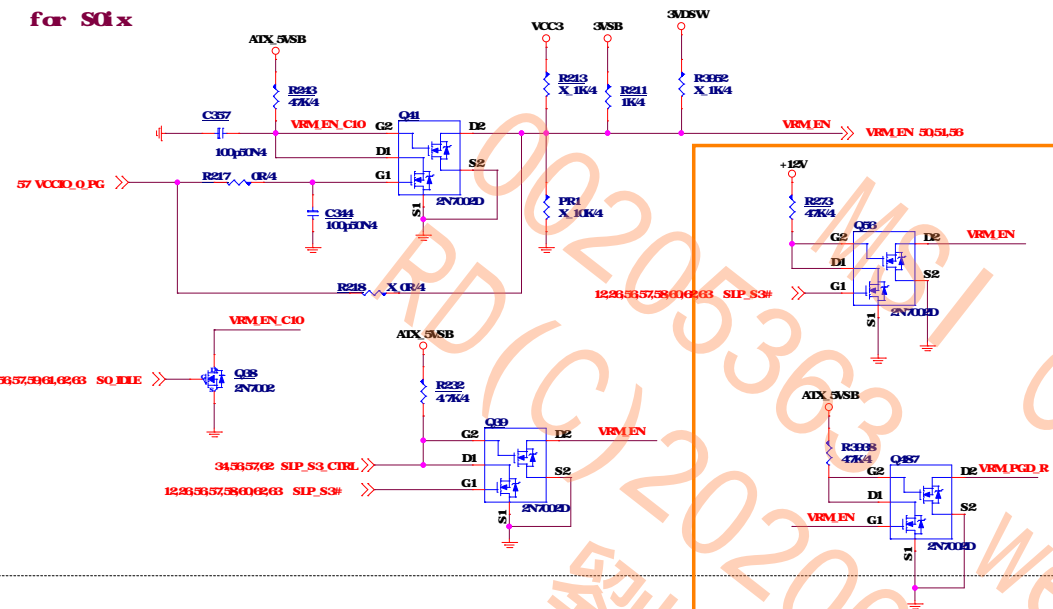


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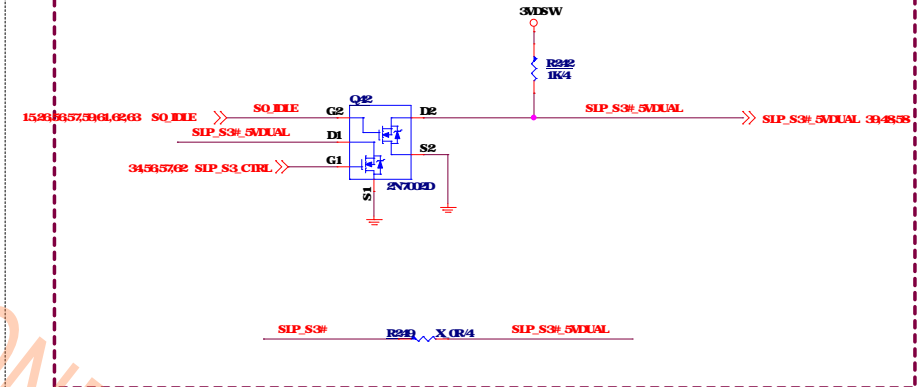
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Size Custom	Document Description DDR FWR VP25VT	Rev 1.1
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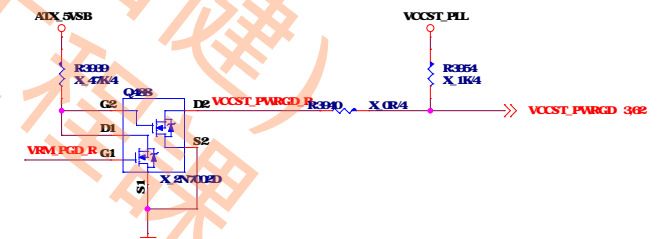
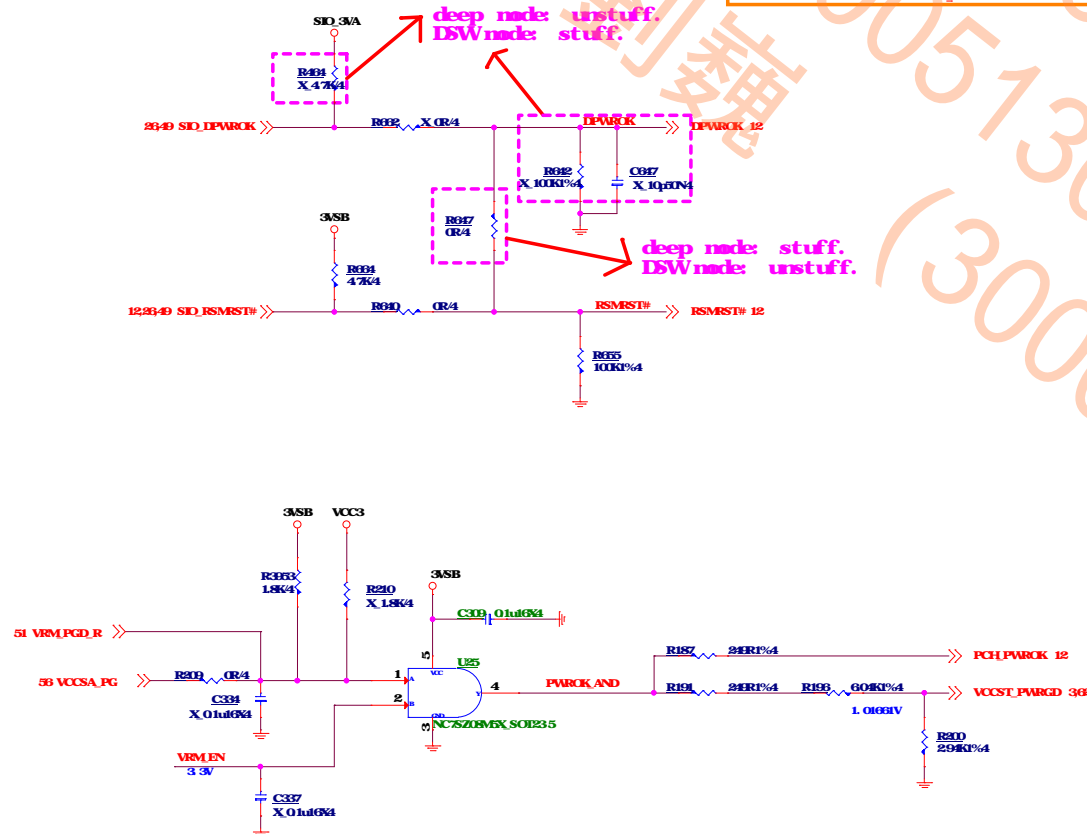
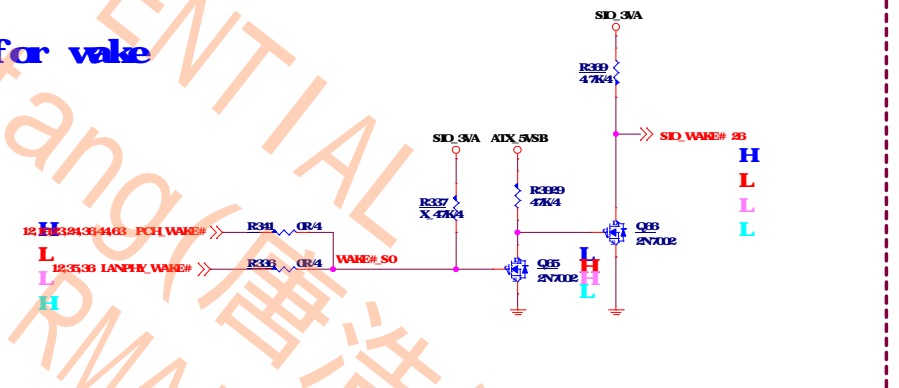
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for $\text{SO}(x)$ 

for 5DIMM and 5DUAL

for $\text{SO}(x)$ 

for wake



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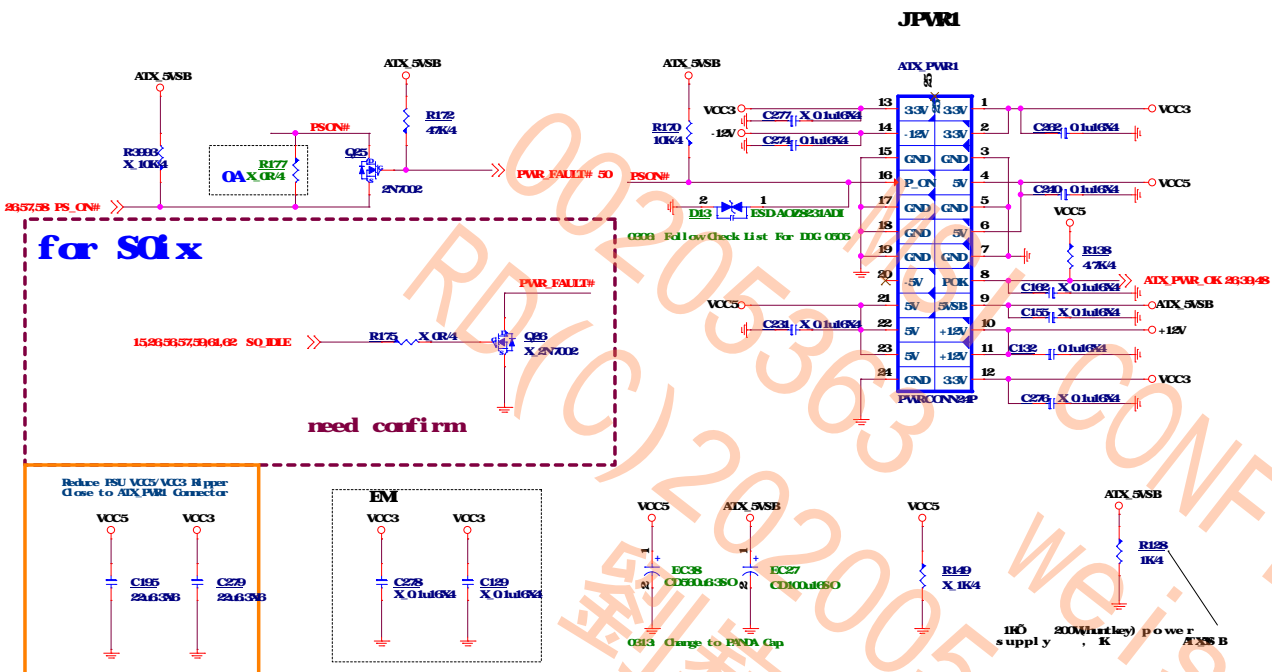
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Size Custom	Document Description POWERSEQUENCE
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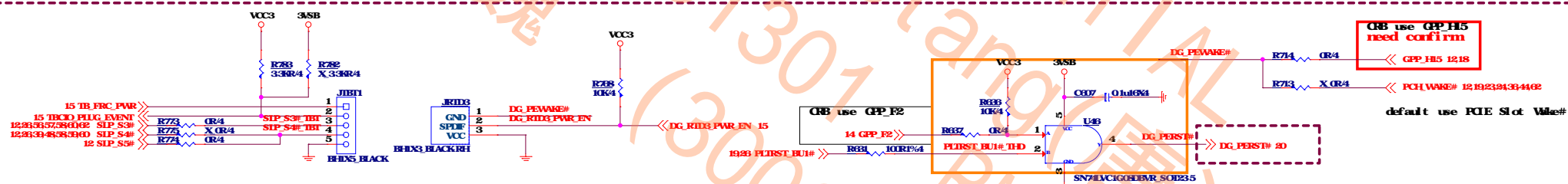
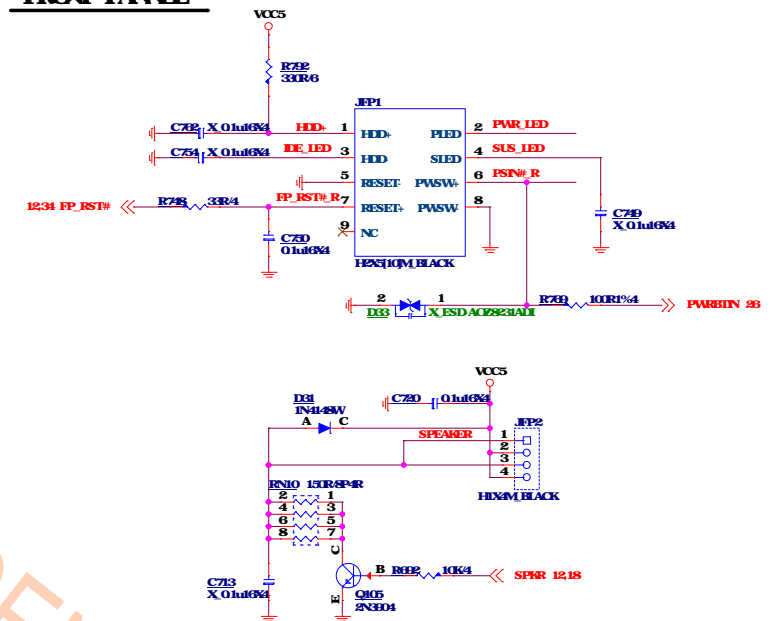
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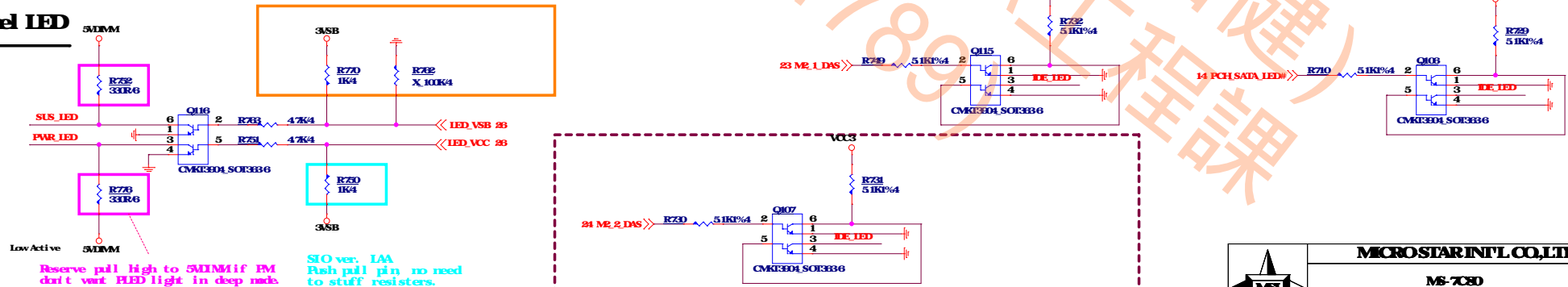
ATX POWER CONNECTOR



FRONT PANNEL



Front Panel LED

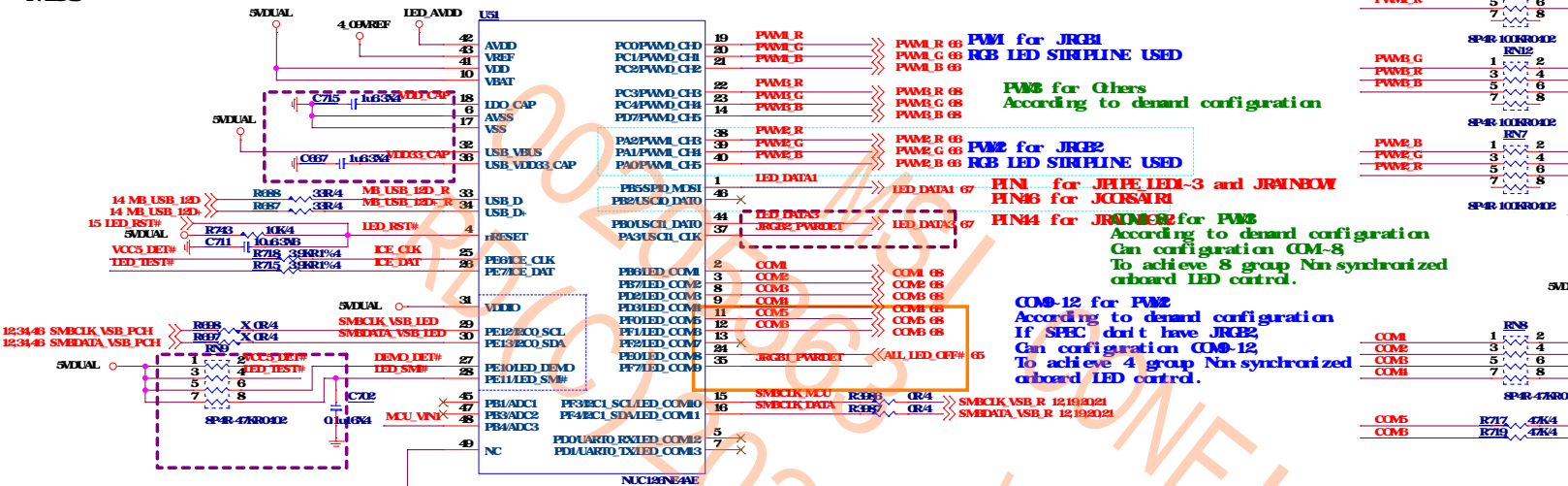


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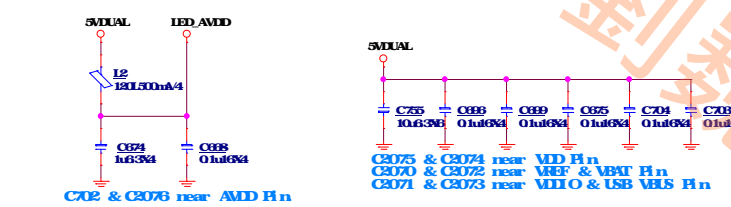
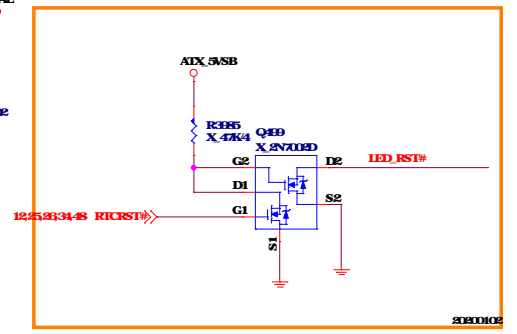
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LED MCU



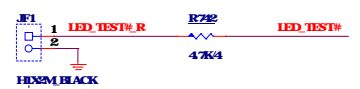
Control	Net Name	PWM USE
PCH	LED_DATA1	No Use
AUDIO Cover	LED_GPIO_01	No Use
MS/IO cover	LED_GPIO_02	No Use
JRAINBOW	LED_GPIO_03	No Use
JCOSAIRI	LED_DATA2	No Use
JRGB/JRGB2	PWM1/ PWM2	PWM1/ PWM2
Board Side LED	COM 1-8	PWM3
Board Side LED	COM 9-16	PWM2



IF no JPVALED1 & JP1PE_LED spec

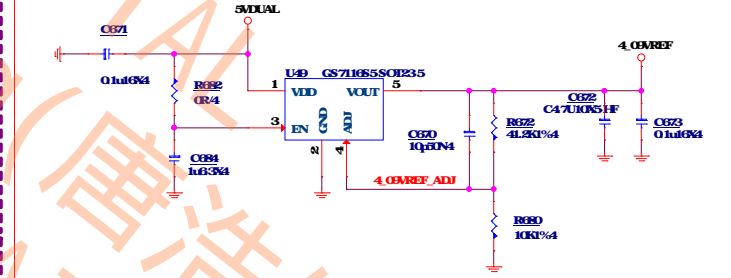
MCU can be powered by 5VDUAL directly.
LED_VCC5 replace with 5VDUAL.

JF1 for Factory test



Check with LED model spec

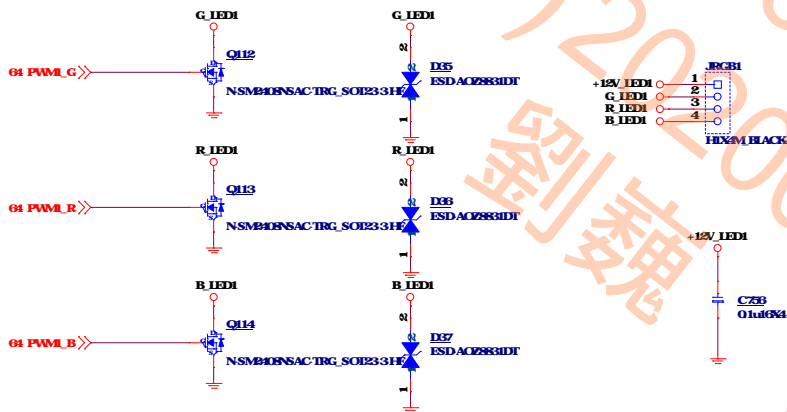
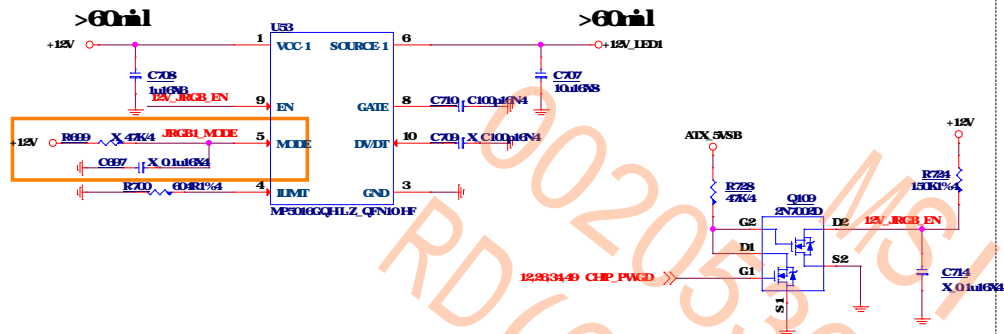
Voltage HW monitor



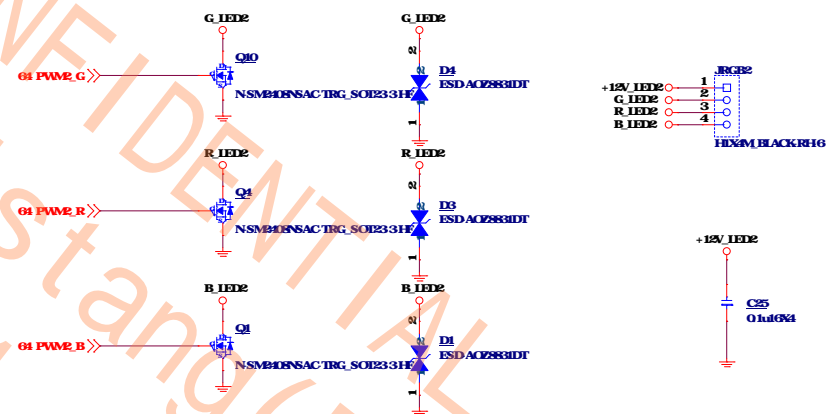
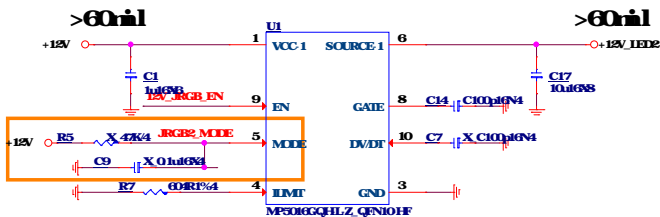
Option spec for voltage monitor require VDI, 2, 3 is example.



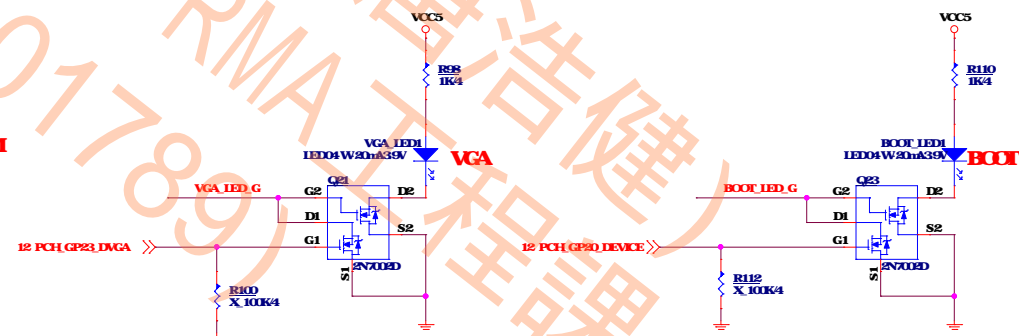
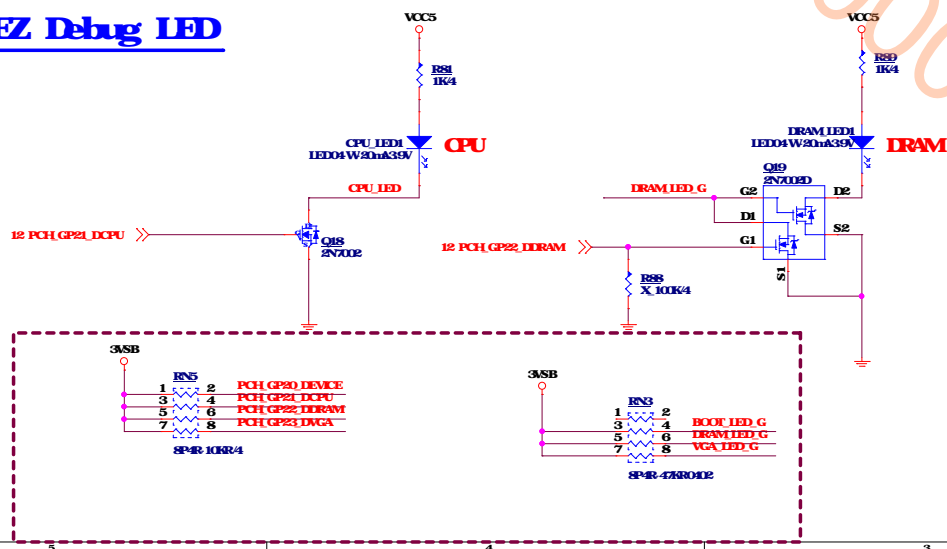
JRGB1



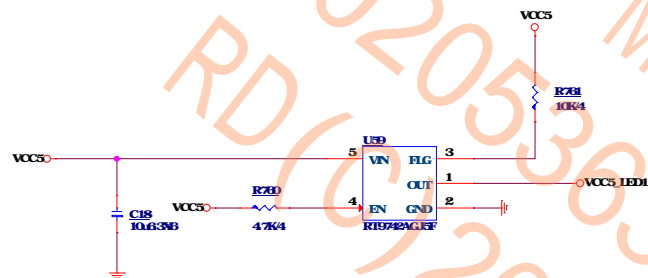
JRGB2



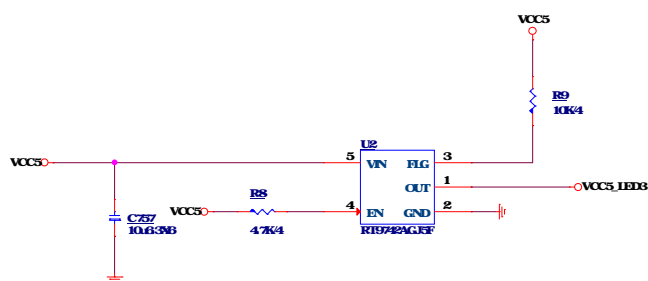
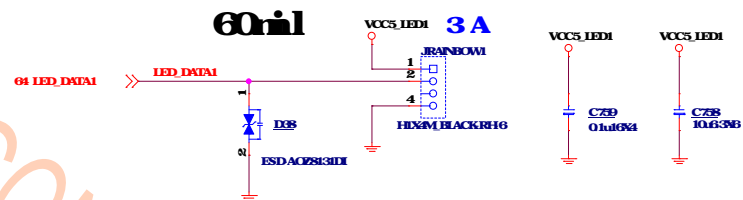
EZ Debug LED



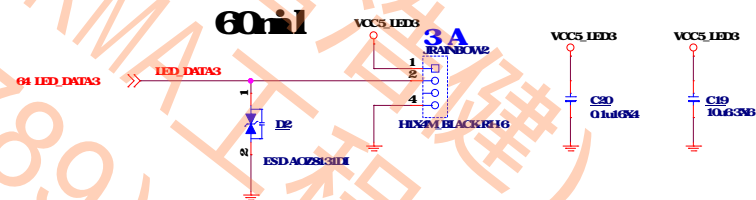
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JRAINBOW1 LED



JRAINBOW2 LED

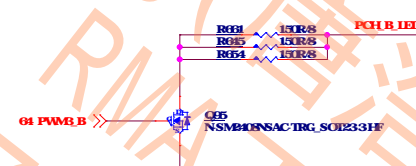
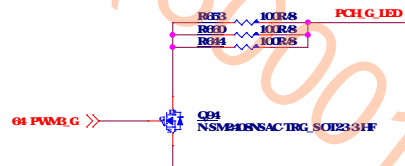
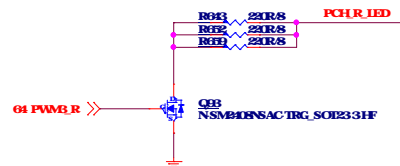
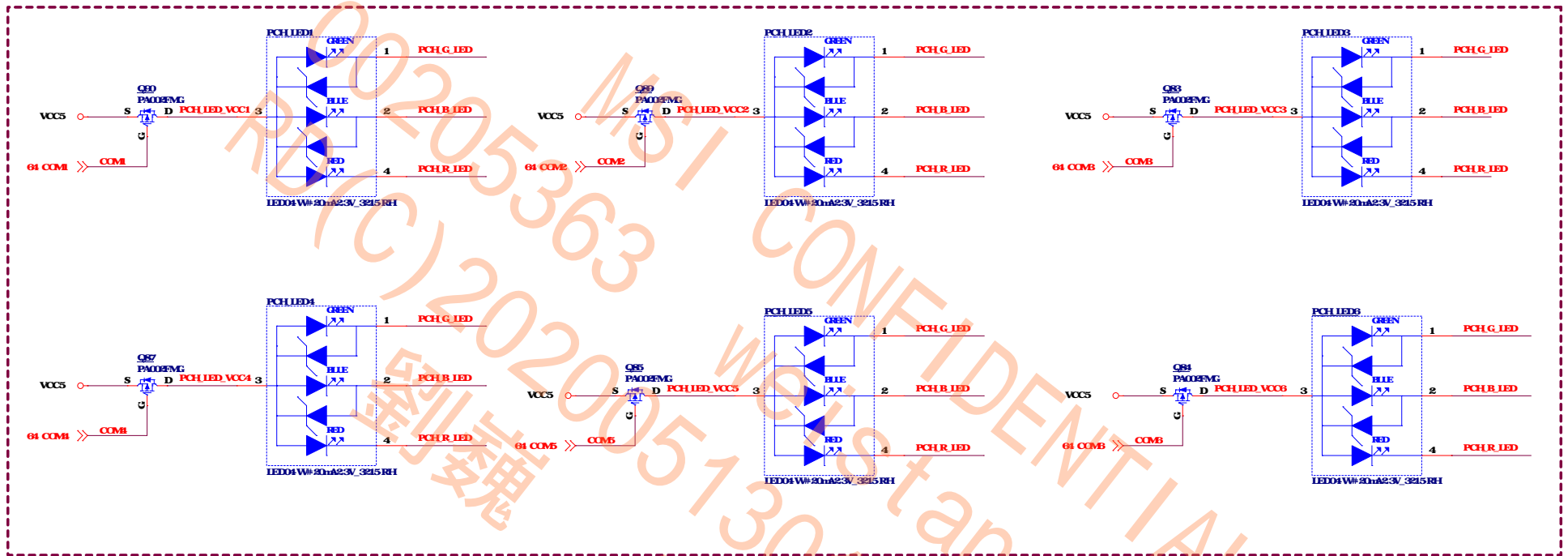


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Custom	JRAINBOW1_2LED	1.1
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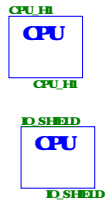
PCH.LED



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Custom	BOARD SIDE LED	1.1	
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708011



Heat Sink

